Design Example Report

Title	***14.5 W Dual Outputs Isolated Flyback Using TinySwitch™-4 TNY289PG***
Specification	85 VAC – 265 VAC Input; 12 V / 1 A, 5 V / 500 mA Output
Application	Appliances and Industrial
Author	Applications Engineering Department
Document Number	DER-881
Date	August 24, 2020
Revision	1.0

Summary and Features

- EcoSmart™ – meets all existing and proposed energy efficiency standards including ErP.
  - > 82% average active-mode efficiency
- The board can fit P/K or the cost-effective D package
- BP/M capacitor values selects power MOSFET current limit for greater design flexibility
- Accurately tolerance I2f parameter (-10%, +12%) reduces system cost
  - Increases MOSFET and magnetics power delivery
  - Reduces overload power, which lowers output diode and capacitors costs
- Integrated TinySwitch-4 safety / reliability features
  - Accurate (±5%), auto-recovering, hysteretic thermal shutdown function maintains safe PCB temperatures under all conditions
  - Auto-restart protects against output short-circuit and open loop fault conditions
  - P and K package with >3.2 mm creepage on package enables reliable operation in high humidity and high pollution environments
- Meets EN550022 and CISPR-22 Class B conducted EMI with >12 dBµV margin
- Meets IEC61000-4-5 Class 3 AC line surge
- No damage during line brown-out or brown-in conditions

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PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes an isolated flyback converter designed to provide a nominal output voltage of 12 V, 1 A and 5 V, 500 mA load from a wide input voltage range of 85 VAC to 265 VAC. This adapter utilizes the TNY289P from the TinySwitch-4 family of ICs, with provision for D and K packages placed on the top layer.

This document contains the complete power supply specifications, bill of materials, transformer construction, circuit schematic and printed circuit board layout, along with performance data and electrical waveforms.

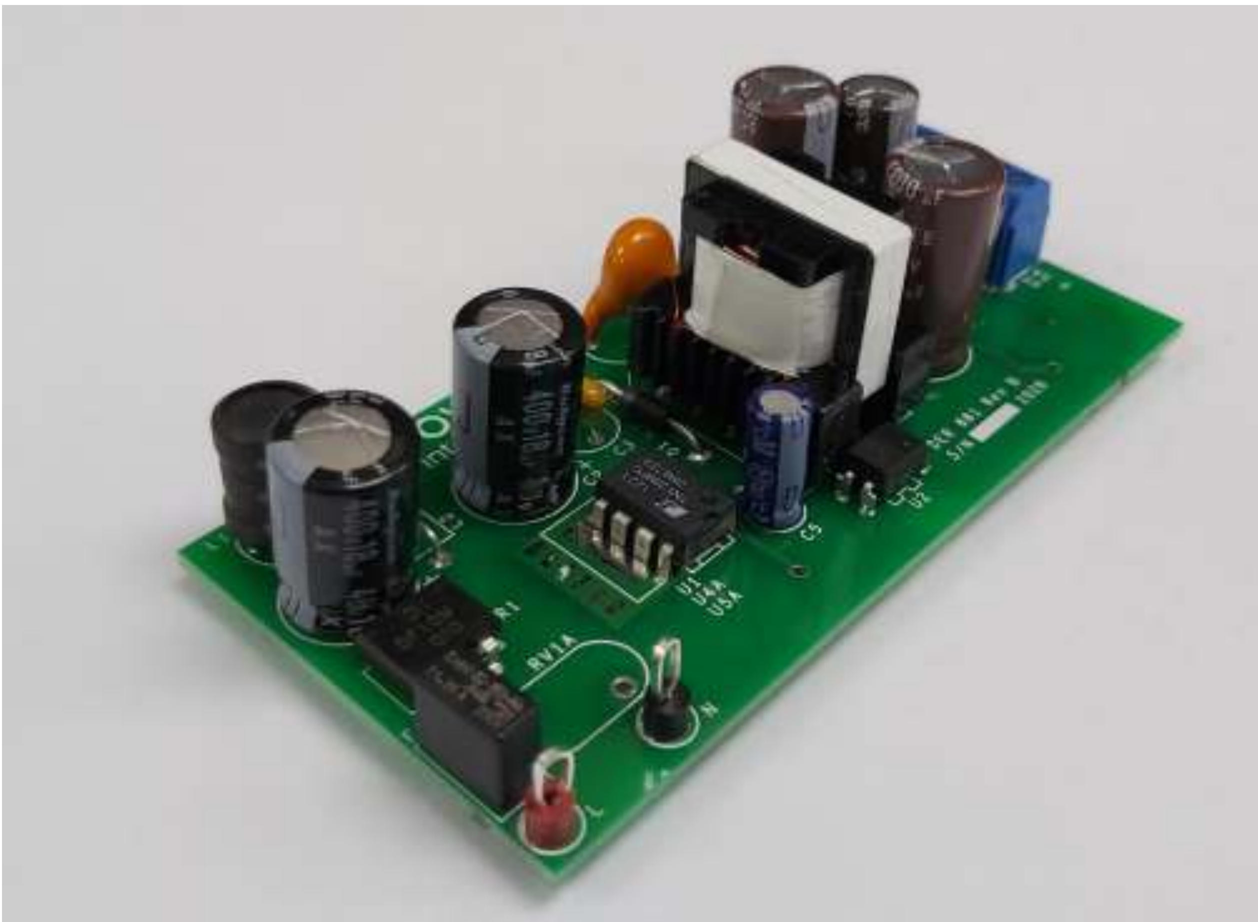

Figure 1 – Populated Circuit Board.

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Figure 2 – Populated Circuit Board, Top View.

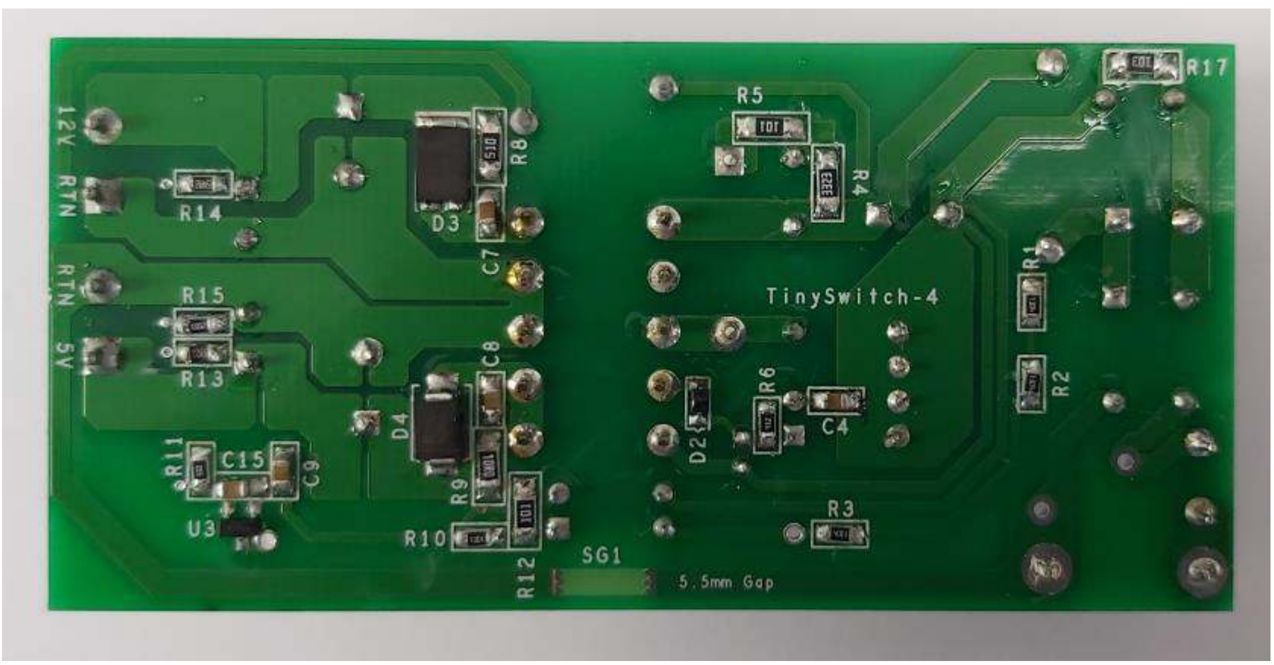

Figure 3 – Populated Circuit Board, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
Output 1						
Output Voltage 1	V_{OUT1}	11	12	13	V	± 8%
Output Ripple Voltage 1	$V_{RIPPLE1}$			150	mV	20 MHz Bandwidth.
Output Current 1	I_{OUT1}	0.1		1	A	± 5%
Output Voltage 2	V_{OUT2}	4.75	5	5.25	V	20 MHz Bandwidth.
Output Ripple Voltage 2	$V_{RIPPLE2}$			50	mV	
Output Current 2	I_{OUT1}	50		500	mA	
Total Output Power						
Continuous Output Power	P_{OUT}			14.5	W	
Efficiency						
Full Load	η	82			%	Measured at P_{OUT} 25 °C
Required average efficiency at 25, 50, 75 and 100 % of P_{OUT}	η_{DOE}	80			%	Per DOE EISA2007 (Level VI) with TNY289 & Standard Current Limit
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Surge (Differential)				1	kV	1.2/50 µs surge, IEC 61000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
Surge (Common mode)				2	kV	
Ring Wave				3	kV	
Electrical Fast Transient				4	kV	
ESD				±15 ±8	kV kV	Air Discharge. Contact Discharge.
Ambient Temperature	T_{AMB}	0		50	°C	Free Convection, Sea Level.

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3 Schematic

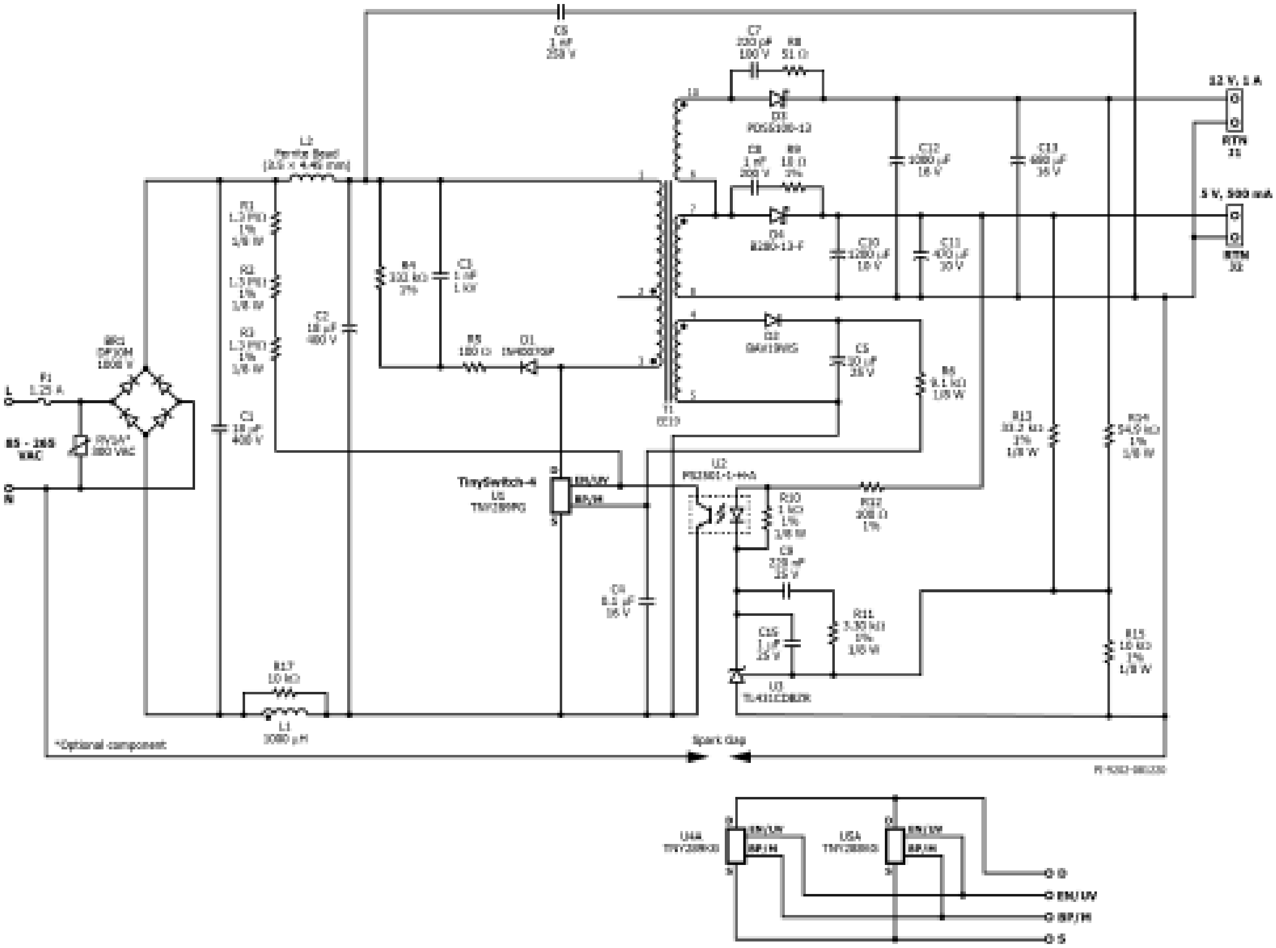

Figure 4 – Schematic.

4 Circuit Description

This circuit is configured as a flyback topology power supply utilizing the TNY289PG. Secondary-side constant voltage (CV) regulation is accomplished through optocoupler feedback with a TL431 reference.

4.1 *Input Rectifier and Filter*

The AC input voltage is rectified by input bridge BR1. The rectified DC is then filtered by the bulk storage capacitors C1 and C2. Inductor L1, L2, C1 and C2 form an input pi filter, which attenuates differential mode conducted EMI.

4.2 *TNY289PG Operation*

The TNY289PG device U1 integrates the power switching device, oscillator, control, startup, and protection functions.

The rectified and filtered input voltage is applied to the primary winding of T1. One side of the power transformer (T1) primary winding is connected to the positive leg of C2, and the other side is connected to the DRAIN (D) pin of U1. At the start of a switching cycle, the controller turns the power MOSFET on and current ramps up in the primary winding, delivering energy from bulk capacitor to transformer. When that current reaches the limit threshold, the controller turns the power MOSFET off. Due to the phasing of the transformer windings and the orientation of the output diode, the stored energy is delivered to the output capacitor during off time.

When the power MOSFET turns off, the leakage inductance of the transformer induces a voltage spike on the drain node. The amplitude of that spike is limited by an RCD clamp network that consists of D1, C3, R4 and R5. Resistor R4 and R5 not only damp the high frequency leakage ring that occurs when the power MOSFET turns off, but also limit the reverse current through D1 when the power MOSFET turns on. This allows a slow, low-cost, glass passivated diode (with a recovery time of $\leq$2 μs.) to be used for D1. The slow diode also improves conducted EMI and efficiency.

Using ON/OFF control, U1 skips switching cycles to regulate the output voltage, based on feedback to its ENABLE/UNDERVOLTAGE (EN/UV) pin. The EN/UV pin current is sampled, just prior to each switching cycle, to determine if that switching cycle should be enabled or disabled. If the EN/UV pin current is <115 μA, the next switching cycle begins, and is terminated when the current through the power MOSFET reaches the internal current limit threshold. To evenly spread switching cycles, preventing group pulsing, the EN/UV pin threshold current is modulated between 115 μA and 75 μA based on the state during the previous cycle. An internal state machine sets the current limit to one of 4 levels appropriate for the operating conditions, ensuring that the switching frequency remains above the audible range until the transformer flux density is low enough to prevent audible noise. This practically eliminates audible noise when standard dip varnishing of the transformer is used.

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4.3 *Output Rectification and Filtering*

Output rectification is provided by D3 and D4 for 12 V and 5 V outputs respectively. Low ESR capacitor C12 and C13 for 12 V output and C10 and C11 for 5 V output achieves minimum output voltage ripple and noise in a small can size for the rated ripple current specification.

4.4 *Feedback and Output Voltage Regulation*

The reference IC, U3 or TL431 is used to set the two output voltages programmed via the resistor div.ider R13, R14 and R15. Both outputs are sensed, and the regulators controls the combination of outputs. A portion of both 12 V and the 5 V outputs are fed into the shunt regulator U3 or TL431. The TL431 varies its cathode voltage in an attempt to keep its input voltage constant (equal to 2.5 V, ±2%). As the cathode voltage changes, the current through the LED and transistor within U3 change. Whenever the EN/UV pin current exceeds its threshold (> 115 µA), the next switching cycle is disabled. Whenever the EN/UV pin current falls below the threshold, the next switching cycle is enabled. As the load is reduced, the number of enabled switching cycles decreases, which lowers the effective switching frequency and the switching losses. This results in almost constant efficiency down to very light loads, which is ideal for meeting energy efficiency requirements. Capacitor C15 rolls off the gain of U3 with frequency, to ensure stable operation.

Good cross-regulation on 12 V and 5 V outputs is achieved by AC-stacked the secondary windings 12 V and 5 V and by sum regulating (obtaining feedback from both outputs).

4.5 *Undervoltage Lockout*

This undervoltage (UV) lockout detection is accomplished by sensing the rectified dc voltage thru resistors R1, R2 and R3. When installed, power MOSFET switching is disabled at start-up until the current into the EN/UV pin exceeds 25 µA. This allows the designer to set the input voltage at which MOSFET switching will be enabled by choosing the sum of R1 – R3. For example, a value of 3.9 MΩ requires an input voltage of 70 VAC (99 VDC across C2) before the current into the EN/UV pin exceeds 25 µA. The UV detect function also prevents the output of the power supply from glitching (trying to restart) after output regulation is lost (during shutdown), by disabling power MOSFET switching until the input voltage rises above the undervoltage lockout threshold.

4.6 *EMI Design Aspects*

In addition to the simple input π filter (C1, L1, C2 and L2) for differential mode EMI, this design makes use of shielding techniques in the transformer to reduce common mode EMI displacement currents. Resistor R4 and capacitor C3 are added to act as damping network to reduce high frequency transformer ringing. These techniques combined with the frequency jitter of TNY289PG gives excellent conducted and radiated EMI performance.

4.7 *ESD Design Aspects*

Component placement and board layout play a crucial role in order to pass ESD compliance requirements. The following design considerations were applied in this reference board:

- Place C4 as close as possible and directly to BP and SOURCE pins.

- Separate the ground trace of U2 from the ground trace of C5. The two ground traces can be merged at the bulk capacitor C2 ground pin. This minimizes coupling of ESD.

- Route Y capacitor C6 traces directly to bulk capacitor C2 positive pin, and the other end to directly to RTN terminal

- Route the spark gap between RTN terminal and Neutral terminal

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5 PCB Layout

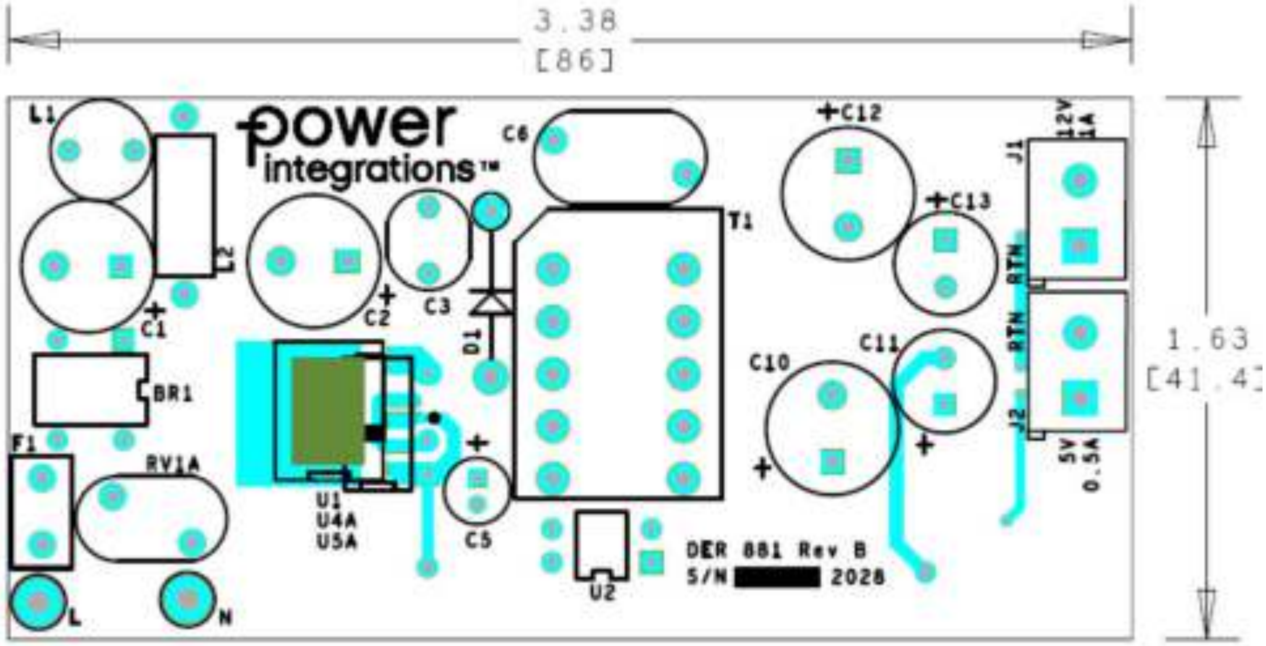

Figure 5 – Top Side.

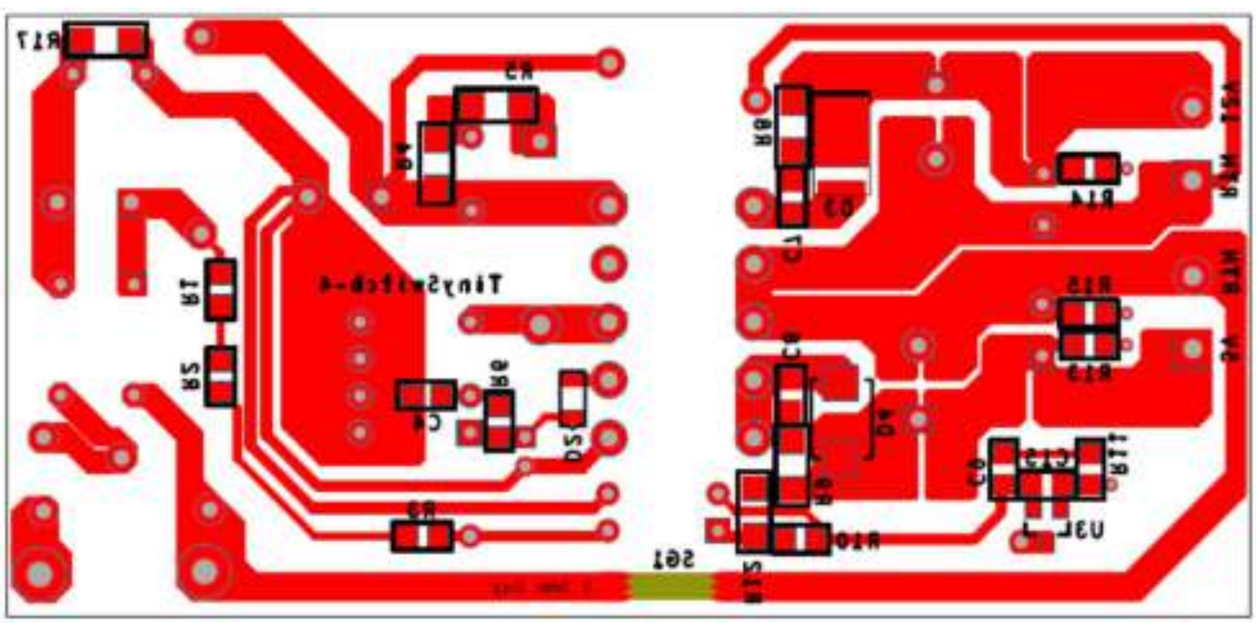

Figure 6 – Bottom Side.

6 Bill of Materials

6.1 *Electrical BOM*

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 1 A, Bridge Rectifier, DF-M, Glass Passivated, 4-EDIP	DF10M	Diodes, Inc.
2	2	C1 C2	18 μF, 20%, 400 V, Electrolytic, Gen. Purpose, (10 x 16 mm), 2000 Hrs @ 105°C	400AX18MEFC10X16	Rubycon
3	1	C3	1 nF, 1 kV, Disc Ceramic, C0G	C330C102JDG5TA	Panasonic
4	1	C4	0.1 μF, ±5%, 16V, X7R, 0805	C0805C104J4RACTU	Kemet
5	1	C5	10 μF, 25 V, Electrolytic, Gen. Purpose, (5 x 12)	ECA-1EM100	Panasonic
6	1	C6	1 nF, Ceramic, Y1	440LD10-R	Vishay
7	1	C7	220 pF, 100 V, Ceramic, X7R, 0805	08051C221KAT2A	AVX
8	1	C8	1 nF, 200 V, Ceramic, X7R, 0805	080552C102KAT2A	AVX
9	1	C9	220 nF, 25 V, Ceramic, X7R, 0805	CC0805KRX7R8BB224	Yageo
10	1	C10	1200 μF, 10 V, Electrolytic, Very Low ESR, 23 mΩ, (10 x 20)	EKZE100ELL122MJ20S	Nippon Chemi-Con
11	1	C11	470 μF, 10 V, Electrolytic, Very Low ESR, 72 mΩ, (8 x 11.5)	EKZE100ELL471MHB5D	Nippon Chemi-Con
12	1	C12	1000 μF, 16 V, Electrolytic, Very Low ESR, 23 mΩ, (10 x 20)	EKZE160ELL102MJ20S	Nippon Chemi-Con
13	1	C13	680 μF, 16 V, Electrolytic, Very Low ESR, 38 mΩ, (8 x 20)	EKZE160ELL681MH20D	Nippon Chemi-Con
14	1	C15	1 μF, ±10%, 25 V, Ceramic, X7R, 0805	GCM21BR71E105KA56L	Murata
15	1	D1	1000 V, 1 A, Rectifier, Glass Passivated, 2 us, DO-41	1N4007GP-E3/54	Vishay
16	1	D2	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
17	1	D3	Diode Schottky 100 V 5 A POWERDI5	PDS5100-13	Diodes, Inc.
18	1	D4	80 V, 2 A, Schottky, SMD, SMB/DO214AA	B280-13-F	Diodes, Inc.
19	1	F1	FUSE, 1.25 A 250 VAC, Slow, 8.35 mm x 4.0 mm x 7.7 mm	RST 1.25-BULK	Bel Fuse
20	1	L1	1000 μH, 0.3 A	RLB0914-102KL	Bourns
21	1	L2	3.5 mm x 4.45 mm, 56 Ω at 100 MHz, #22 AWG hole, Ferrite Bead	2761001112	Fair-Rite
22	3	R1 R2 R3	RES, 1.3 MΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1304V	Panasonic
23	1	R4	RES, 332 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF3323V	Panasonic
24	1	R5	RES, 100 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ101V	Panasonic
25	1	R6	RES, 9.1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ912V	Panasonic
26	1	R8	RES, 51 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ510V	Panasonic
27	1	R9	RES, 10 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF10R0V	Panasonic
28	1	R10	RES, 1.00 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1001V	Panasonic
29	1	R11	RES, 3.30 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3301V	Panasonic
30	1	R12	RES, 100 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1000V	Panasonic
31	1	R13	RES, 33.2 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3322V	Panasonic
32	1	R14	RES, 54.9 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF5492V	Panasonic
33	1	R15	RES, 10.0 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1002V	Panasonic
34	1	R17	RES, 10 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ103V	Panasonic
35	1	T1	Bobbin, EE19, Vertical, 10 pins	TF-1932	Shulin Enterprise
36	1	U1	TinySwitch-4, DIP-8C	TNY289PG	Power Integration
37	1	U2	Optocoupler, 80 V, CTR 80-160%, 4-DIP	PS2501-1-H-A	CEL
38	1	U3	IC, Shunt Regulator Adj.,2.495 V, 2.2%, 100 mA, 0°C ~ 70°C (TA), SOT23-3, TO-236-3, SC-59, SOT-23-3	TL431CDBZR	Texas Instruments

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6.2 *Mechanical BOM*

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	J1 J2	CONN TERM BLOCK, 2 POS, 5mm, PCB	ED500/2DS	On Shore Tech
2	1	L	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
3	1	N	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone

7 Transformer Specification

7.1 *Electrical Diagram*

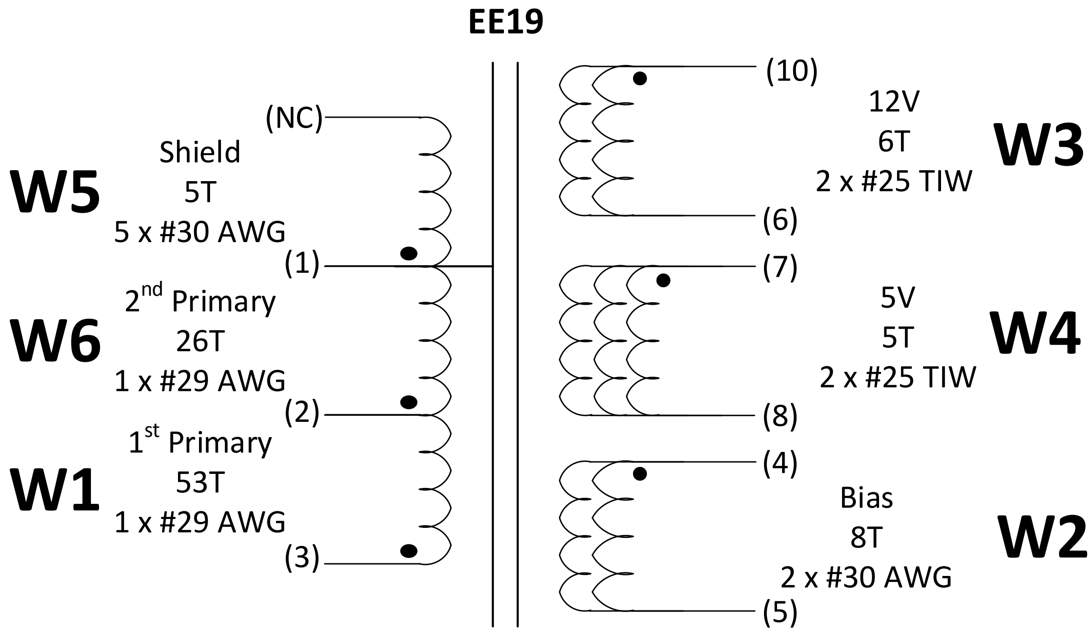

Figure 7 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 3 and pin 1.	770 μH
Tolerance	Tolerance of Primary Inductance.	±5%
Leakage Inductance	Measured across primary winding with all other windings shorted.	<30 μH

7.3 *Material List*

Item	Description
[1]	Core: EE19 PC44.
[2]	Bobbin: EE19, Vertical, 10 Pins. PI#: 25-00969-00.
[3]	Magnet Wire: #29 AWG.
[4]	Magnet Wire: #30 AWG.
[5]	Tripe Insulated Wire: #25.
[6]	Polyester Tape: 9 mm.
[7]	Polyester Tape: 5 mm.
[8]	Varnish: Dolph BC 359 or equivalent.
[9]	Bus wire: #28 AWG, Alpha Wire, Tinned Copper,

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7.4 *Transformer Build Diagram*

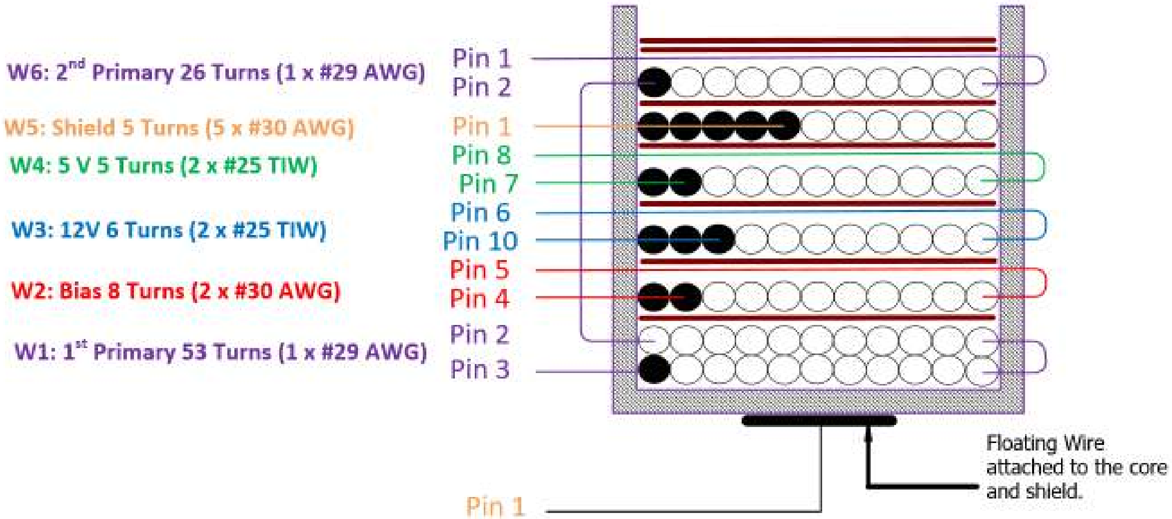
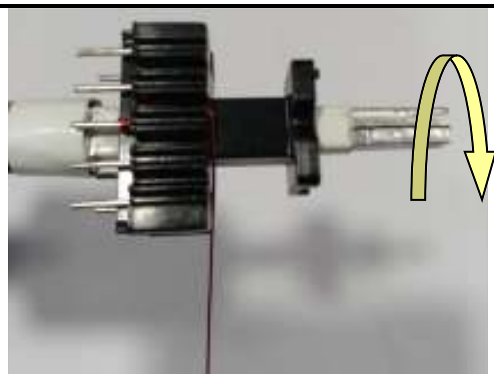
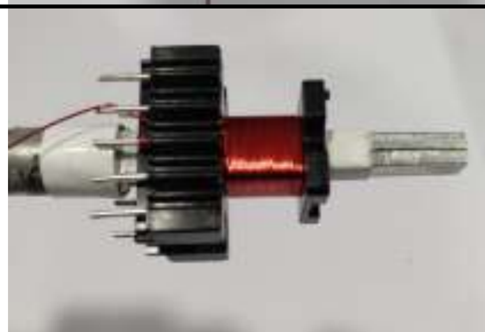
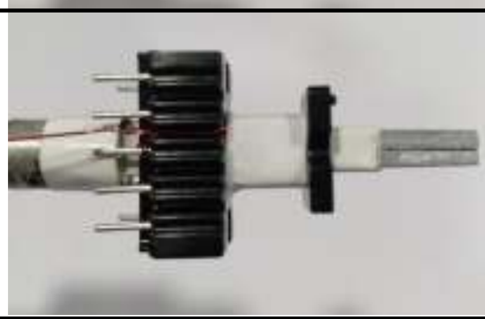


Figure 8 – Transformer Build Diagram.

7.5 *Transformer Construction*

Winding Preparation	Place the bobbin Item [2] with the pins facing the winder. Winding direction is counter-clockwise as shown.
W1 1st Primary	Start at pin 3. Wind 53 turns of wire Item [3] in two layers. After the last turn, bring the wire back across the windings into pin 2.
Insulation	Place one layer of tape Item [6] for insulation.
W2 Bias	Start at pin 4. Wind 8 turns of two strands of wire Item [4] in one layer. Wind all turns on tightly on one side. Bring the back into pin 5.
Insulation	Place one layer of tape Item [6] for insulation.
W3 12 V Secondary	Start at pin 10. Wind 6 turns of two strands of wire Item [5] in one layer. Finish at pin 6.
Insulation	Place one layer of tape Item [6] for insulation.
W4 5 V Secondary	Start at pin 7. Wind 5 turns of two strands of wire Item [5] in one layer. Finish at pin 8.
Insulation	Place one layer of tape Item [6] for insulation
W5 Shield	Start at pin 1. Wind 5 turns of five strands of wire Item [4] in one layer. Spread the turns evenly across the bobbin. The end of the last turn is no-connect (NC).
Insulation	Place one layer of tape Item [6] for insulation
W6 2nd Primary	Start at pin 2. Wind 26 turns of wire Item [3] in one layer. After the last turn, bring the wire back across the windings into pin 1.
Insulation	Place two layer of tape Item [6] for insulation
Assembly	Grind core halves for specified primary inductance. Place a floating wire Item [9] along the core, and solder one end to pin 1. Wrap core halves and floating wire with tape Item [7]. Do not Remove pin 2 and pin 9. Varnish with Item [8].

7.6 *Winding Illustrations*

Winding Preparation		Place the bobbin Item [2] with the pins facing the winder. Winding direction is counter-clockwise as shown.
W1 1st Primary		Start at pin 3. Wind 53 turns of wire Item [3] in two layers. End at pin 2.
Insulation		Place one layer of tape Item [6] for insulation.

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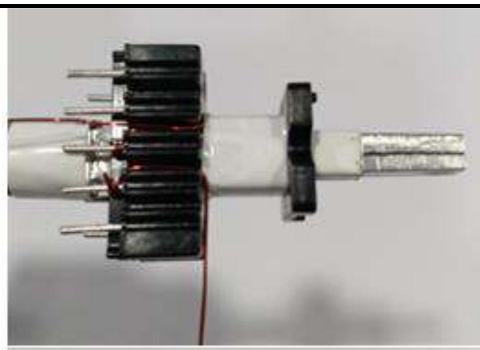
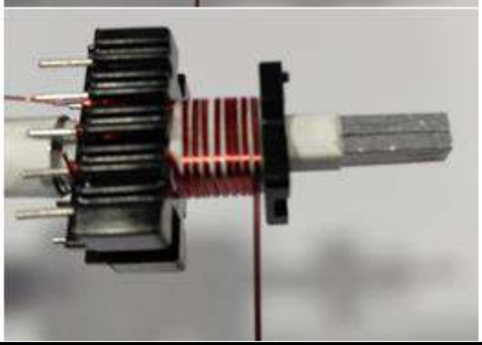
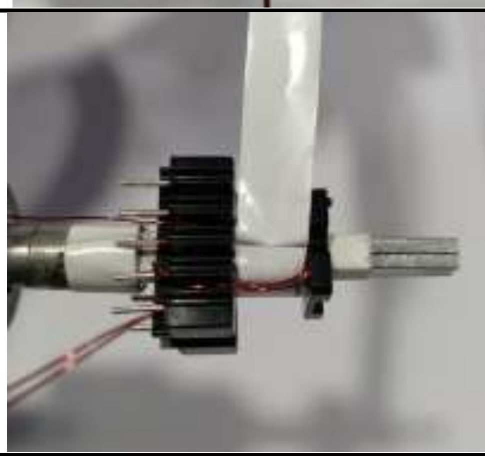
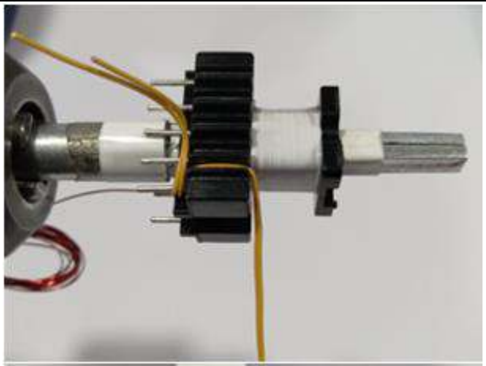
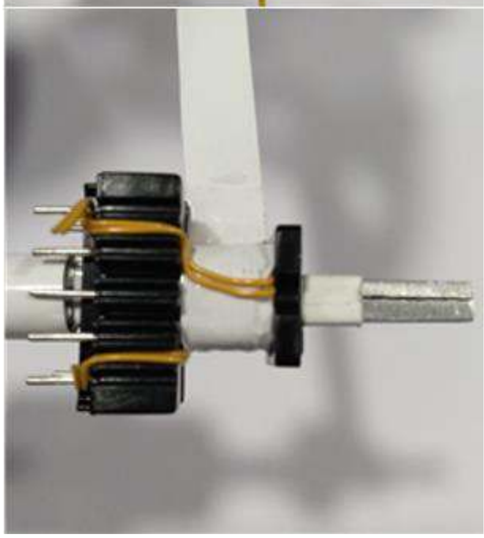
W2 **Bias**		Start at pin 4. Wind 8 turns of two strands of wire Item [4] in one layer. Wind all turns on tightly on one side. Bring the back into pin 5.
Insulation		Place one layer of tape Item [6] for insulation.

W3 **12V** **Secondary**	 	Start at pin 10. Wind 6 turns of two strands of wire Item [5] in one layer. Finish at pin 6.
Insulation		Place one layer of tape Item [6] for insulation.

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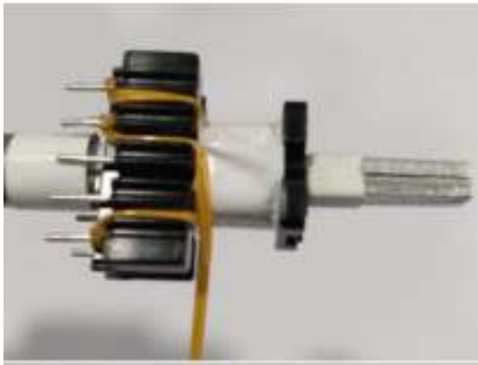
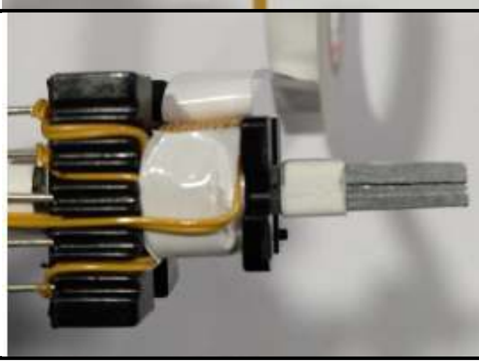
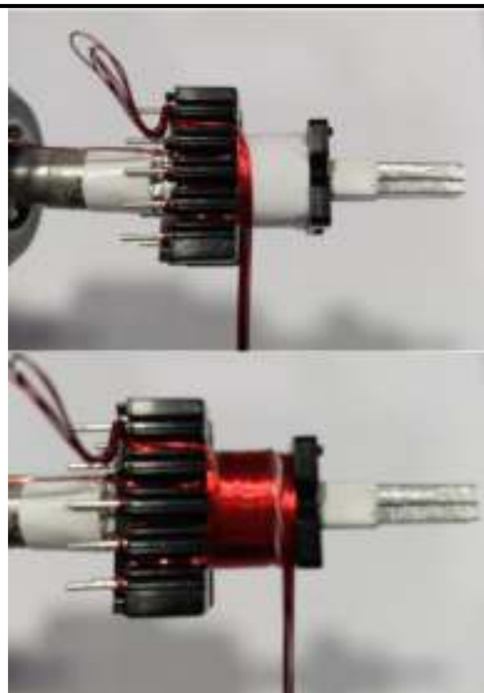
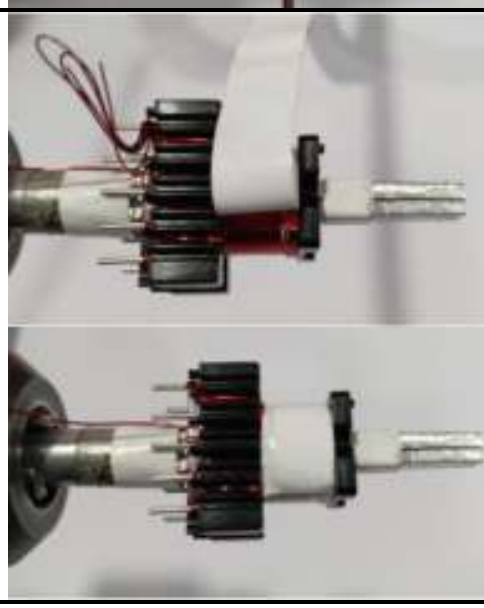
W4 5V Secondary	 	Start at pin 7. Wind 5 turns of two strands of wire Item [5] in one layer. Finish at pin 8.
Insulation		Place one layer of tape Item [6] for insulation.

W5 Shield		Start at pin 1. Wind 5 turns of five strands of wire Item [4] in one layer. Spread the turns evenly across the bobbin. The end of the last turn is no connect (NC).
Insulation		Place one layer of tape Item [6] for insulation

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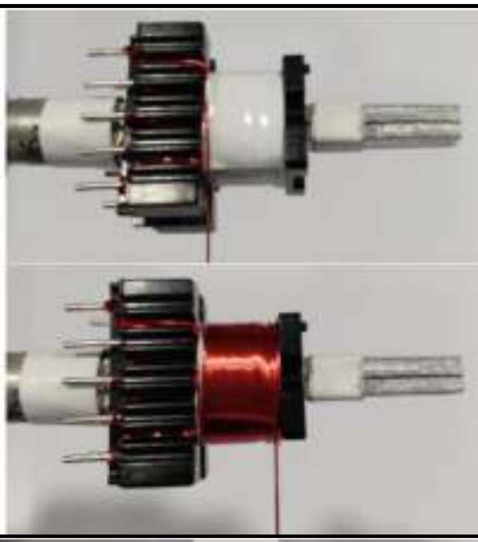
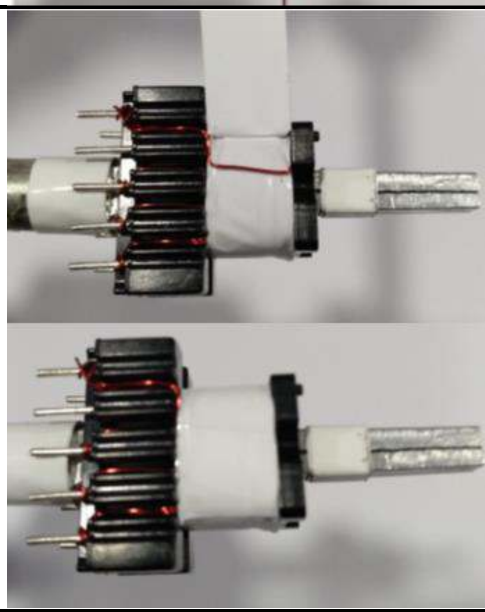
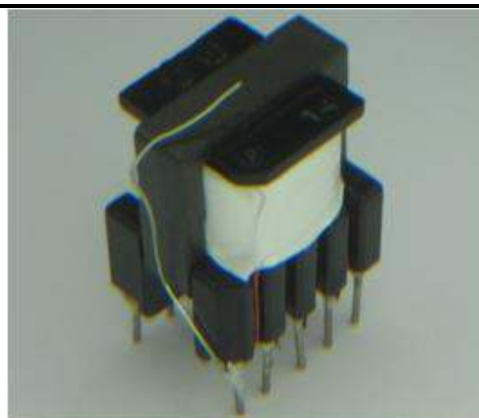
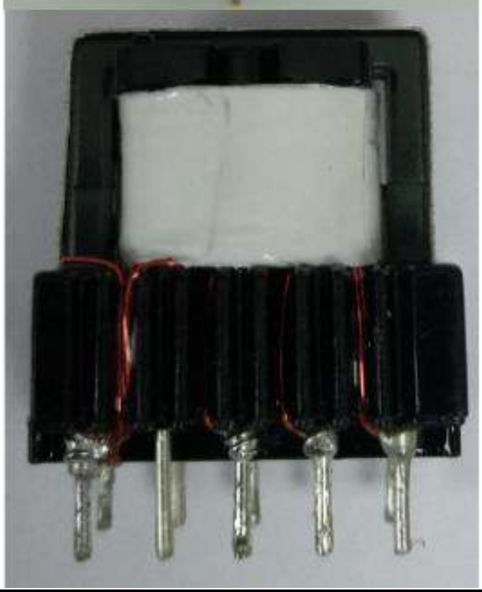
W6 **2nd Primary**		Start at pin 2. Wind 26 turns of wire Item [3] in one layer. After the last turn, bring the wire back across the windings into pin 1.
Insulation		Place two layers of tape Item [6] for insulation

Assembly	 	Grind core halves for specified primary inductance. Place a floating wire Item [9] along the core, and solder one end to pin 1. Wrap core halves and floating wire with tape Item [7]. Do not Remove pin 2 and pin 9. Varnish with Item [8].

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8 Transformer Design Spreadsheet

8.1 *TinySwitch4 Design Spreadsheet*

ACDC_TinySwitch-4_110618; Rev.1.2; Copyright Power Integrations 2018	INPUT	INFO	OUTPUT	UNIT	ACDC_TinySwitch-4_110618_Rev1-2.xls; TinySwitch-4 Continuous / discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85		85	Volts	Minimum AC Input Voltage
VACMAX	265		265	Volts	Maximum AC Input Voltage
fL	50		50	Hertz	AC Mains Frequency
VO	12.00		12.00	Volts	Output Voltage (at continuous power)
IO	1.20		1.20	Amps	Power Supply Output Current (corresponding to peak power)
Power			14.40	Watts	Continuous Output Power
n	0.83		0.83		Efficiency Estimate at output terminals. Under 0.7 if no better data available
Z	0.50		0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	36.00		36.00	uFarads	Input Capacitance
ENTER TinySwitch-4 VARIABLES					
TinySwitch-4	TNY289P		TNY289P		User-defined TinySwitch-4
Chose Configuration	STD		Standard Current Limit		Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.605	Amps	Minimum Current Limit
ILIMITTYP			0.65	Amps	Typical Current Limit
ILIMITMAX			0.695	Amps	Maximum Current Limit
fSmin			124000	Hertz	Minimum Device Switching Frequency
I^2fmin			50.193	A^2kHz	I^2f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	100.0		100.0	Volts	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10.0	Volts	TinySwitch-4 on-state Drain to Source Voltage
VD			0.70	Volts	Output Winding Diode Forward Voltage Drop
KP			0.79		Ripple to Peak Current Ratio (KP < 6)
KP_TRANSIENT			0.44		Transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER BIAS WINDING VARIABLES					
VB	10.00		10.00	Volts	Bias Winding Voltage
VDB			0.70	Volts	Bias Winding Diode Forward Voltage Drop
NB			8.00		Bias Winding Number of Turns
VZOV			16.00	Volts	Over Voltage Protection zener diode voltage.
UVLO VARIABLES					
V_UV_TARGET			96.54	Volts	Target DC under-voltage threshold, above which the power supply with start
V_UV_ACTUAL			99.70	Volts	Typical DC start-up voltage based on standard value of RUV_ACTUAL
RUV_IDEAL			3.77	Mohms	Calculated value for UV Lockout resistor
RUV_ACTUAL			3.90	Mohms	Closest standard value of resistor to RUV_IDEAL
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EE19		EE19		Enter Transformer Core
Core		EE19		P/N:	PC40EE16-Z
Custom core				P/N:	EE16_BOBBIN
AE			0.23	cm^2	Core Effective Cross Sectional Area
LE			3.94	cm	Core Effective Path Length
AL			1250	nH/T^2	Ungapped Core Effective Inductance

BW			9.0	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3		3		Number of Primary Layers
NS	11		11		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			87.8	Volts	Minimum DC Input Voltage
VMAX			374.8	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.56		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG			0.22	Amps	Average Primary Current
IP			0.61	Amps	Minimum Peak Primary Current
IR			0.48	Amps	Primary Ripple Current
IRMS			0.34	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			774	uHenries	Typical Primary Inductance. +/- 10% to ensure a minimum primary inductance of 774 uH
LP_TOLERANCE	10		10	%	Primary inductance tolerance
NP			79		Primary Winding Number of Turns
ALG			125	nH/T^2	Gapped Core Effective Inductance
BM			2970	Gauss	Maximum Operating Flux Density, BM<3100 is recommended
BAC			1180	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1704		Relative Permeability of Ungapped Core
LG			0.21	mm	Gap Length (Lg > 0.1 mm)
BWE			27	mm	Effective Bobbin Width
OD			0.343	mm	Maximum Primary Wire Diameter including insulation
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.29	mm	Bare conductor diameter
AWG			30	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			102	Cmils	Bare conductor effective area in circular mils
CMA			302	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			4.76	Amps	Peak Secondary Current
ISRMS			2.33	Amps	Secondary RMS Current
IRIPPLE			2.00	Amps	Output Capacitor RMS Ripple Current
CMS			467	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			23	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			605	Volts	Maximum Drain Voltage Estimate (Assumes 20% zener clamp tolerance and an additional 10% temperature tolerance)
PIVS			60	Volts	Output Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1	12.00		12.00	Volts	Main Output Voltage (if unused, defaults to single output design)
IO1	1.00		1.00	Amps	Output DC Current
PO1			12	Watts	Output Power
VD1			0.70	Volts	Output Diode Forward Voltage Drop
NS1			10.00		Output Winding Number of Turns
ISRMS1			2.334	Amps	Output Winding RMS Current
IRIPPLE1			2.00	Amps	Output Capacitor RMS Ripple Current
PIVS1			60	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diodes			1N5820,		Recommended Diodes for this output

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			SB320		
CMS1			467	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			23	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.58	mm	Minimum Bare Conductor Diameter
ODS1			0.90	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2	5.00			Volts	Output Voltage
IO2	0.5			Amps	Output DC Current
PO2			2.5	Watts	Output Power
VD2			0.70	Voltas	Output Voltage Forward Voltage Drop
NS2			4.49		Output Winding Number of Turns
ISRMS2			0.973	Amps	Output Winding RMS Current
IRIPPLE2			0.83	Amps	Output Capacitor RMS Ripple Current
PIVS2			26	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diode			1N5817 SB120		Recommended Diodes for this output
CMS2			195	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			27	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			0.36	mm	Minimum Bare Conductor Diameter
ODS2			2.01	mm	Maximum Outside Diameter for Triple Insulated Wire

Note: All warnings were verified on actual bench tests and passed the criteria specified on the spreadsheet.

9 Performance Data

All measurements were performed at room temperature at 300 s soak time.

9.1 *Efficiency*

9.1.1 Active Mode Measurement Data

Measured Performance			
		V_{IN} (VAC)	
		115	230
		Efficiency (%)	
Load (%)	**10**	79.88	77.45
	25	83.52	79.38
	50	84.50	84.57
	75	84.57	84.68
	100	84.13	84.81
	Ave	**84.18**	**83.36**

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9.1.2 Full Load Efficiency vs. Line

Test Condition: Soak for 15 minutes for each line.

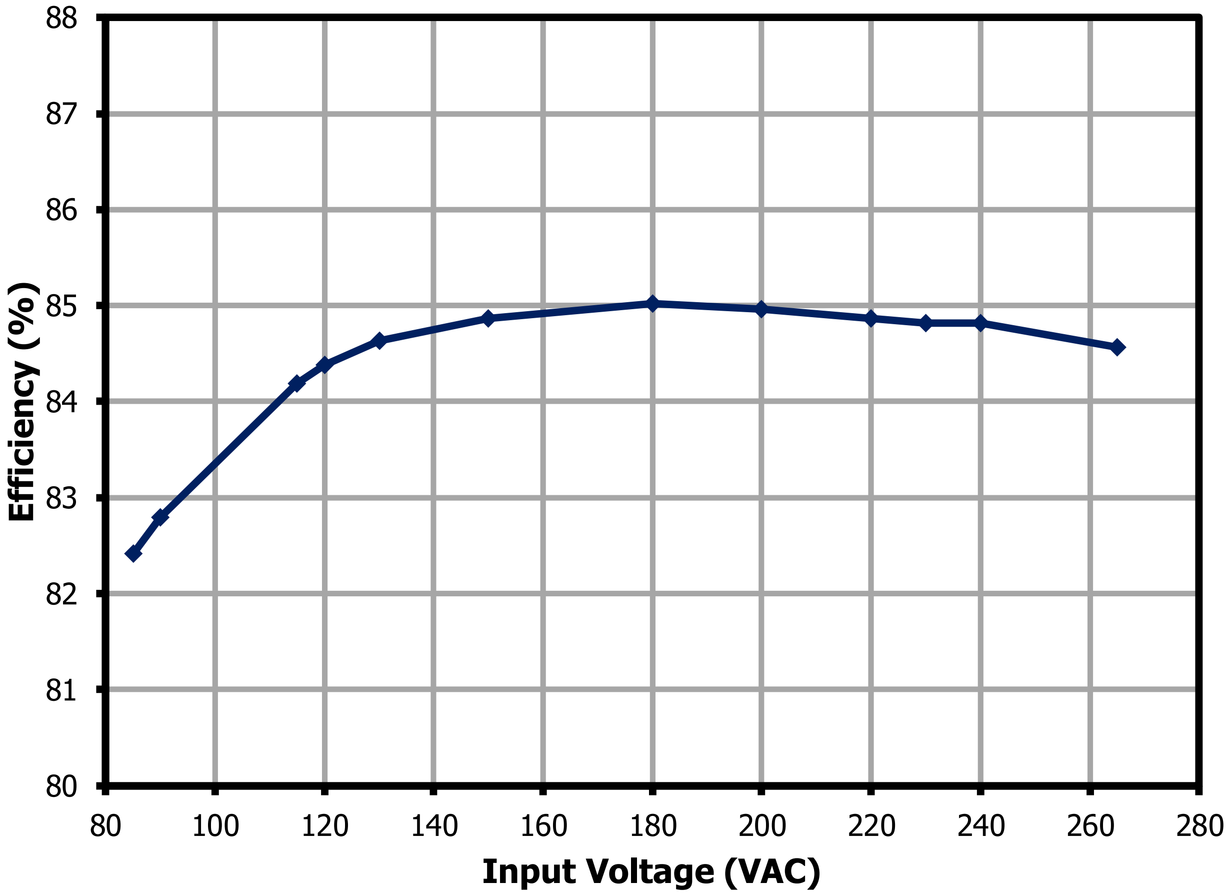

Figure 9 – Full Load Efficiency vs. Line.

9.1.3 Efficiency vs. Load

Test Condition: Soak for 15 minutes each line, and 5 minutes for each load.

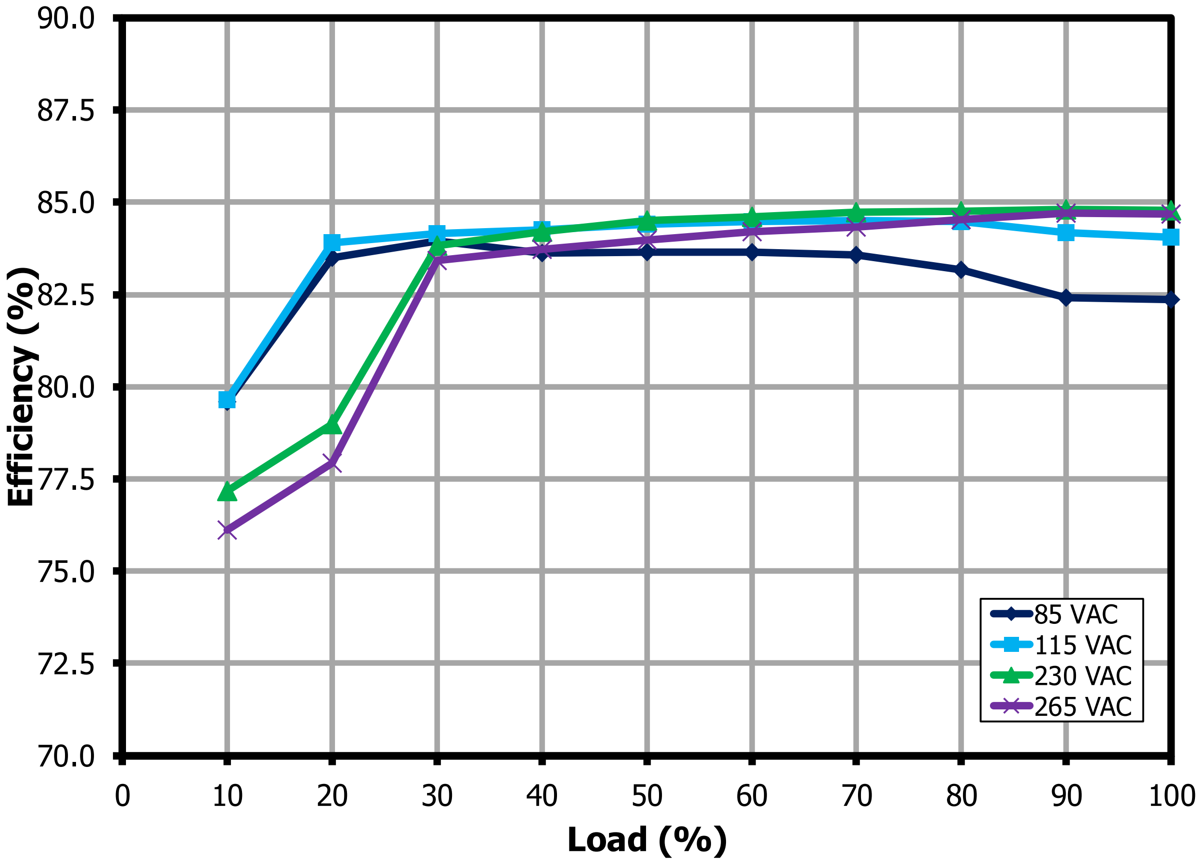

Figure 10 – Efficiency vs. Percentage Load.

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9.2 *Available Standby Output Power*

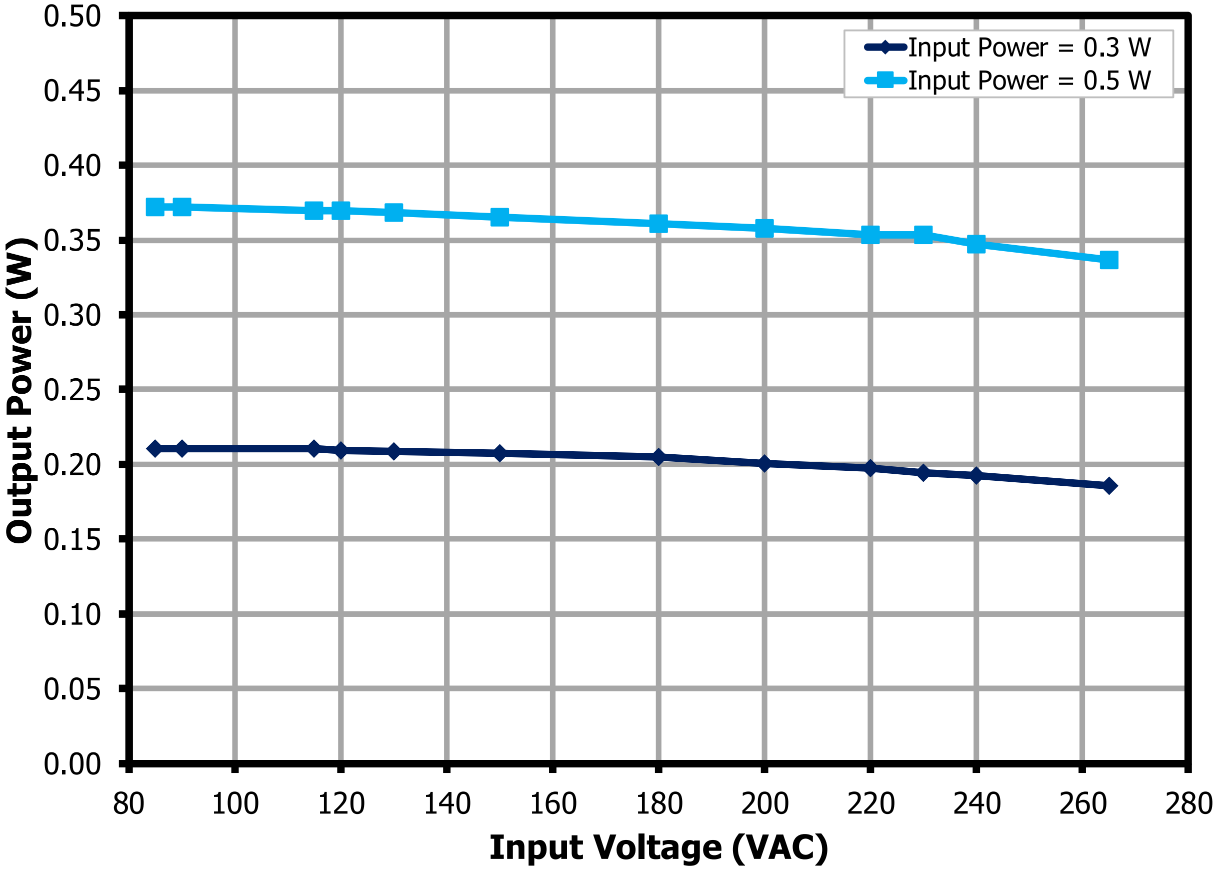

Figure 11 – Available Standby Output Power for 0.3 W and 0.5 W Input Power.

9.3 *Line Regulation*

Test Condition: Soak for 15 minutes for each line.

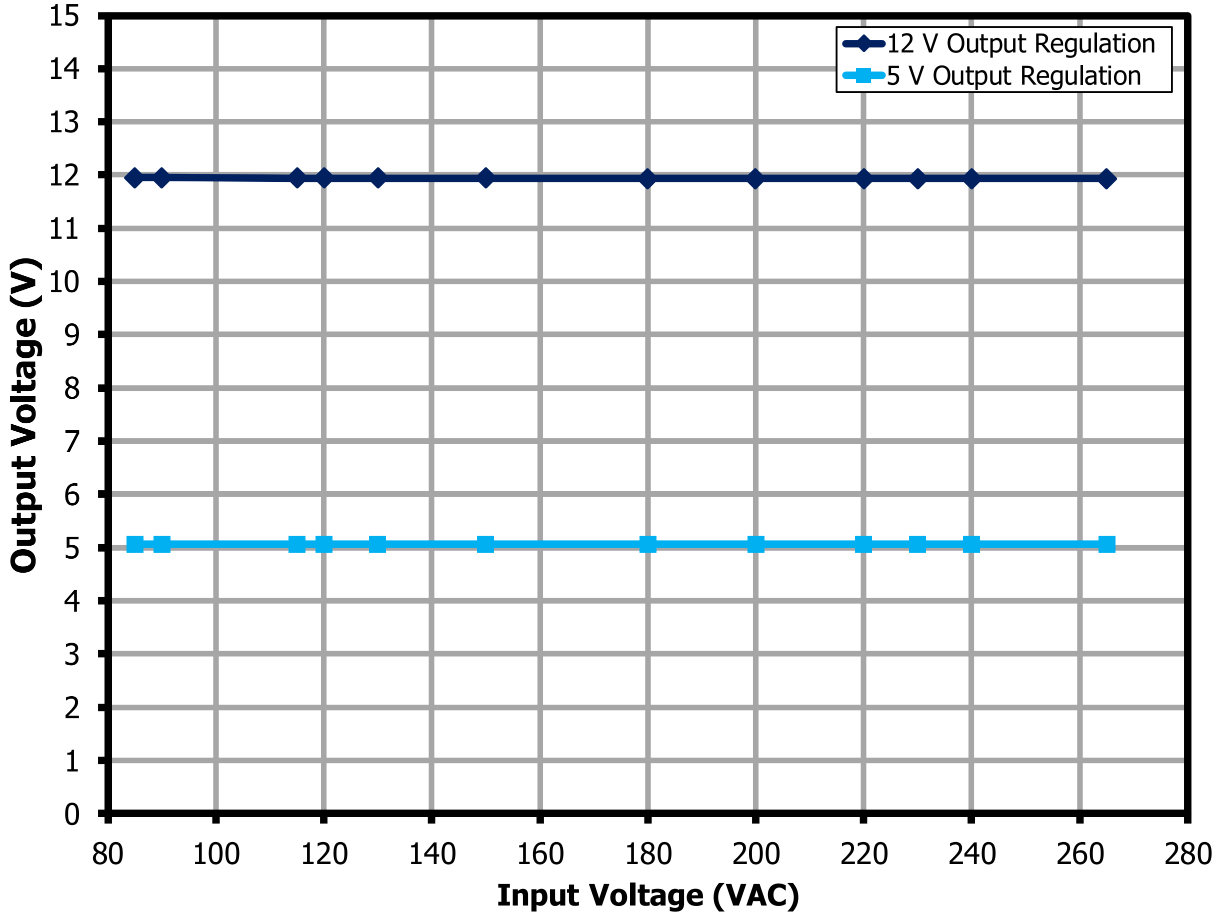

Figure 12 – Output Voltage vs. Line Voltage.

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9.4 *Load Regulation*

Test Condition: Soak for 15 minutes each line, and 5 minutes for each load.

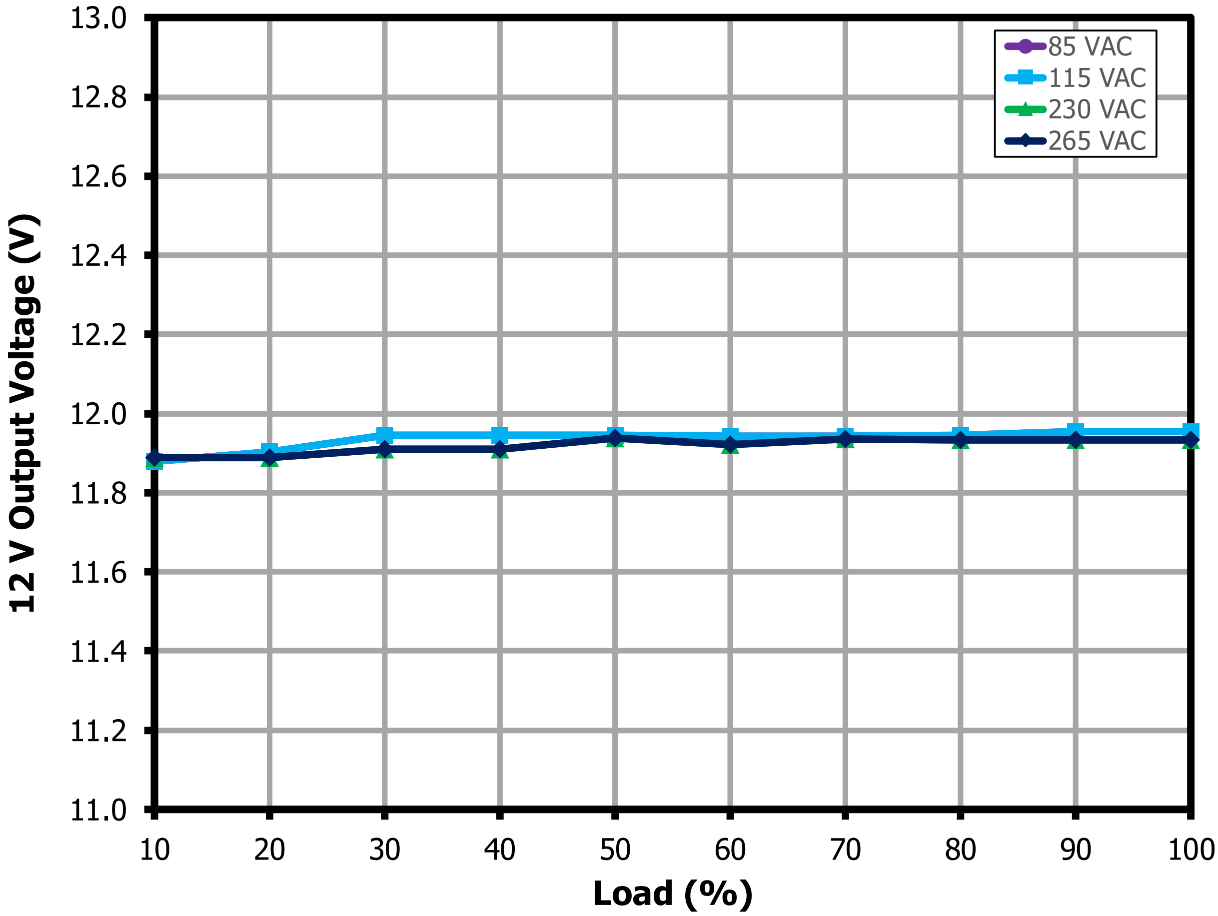

Figure 13 – 12 V Output Voltage vs. Percent Load.

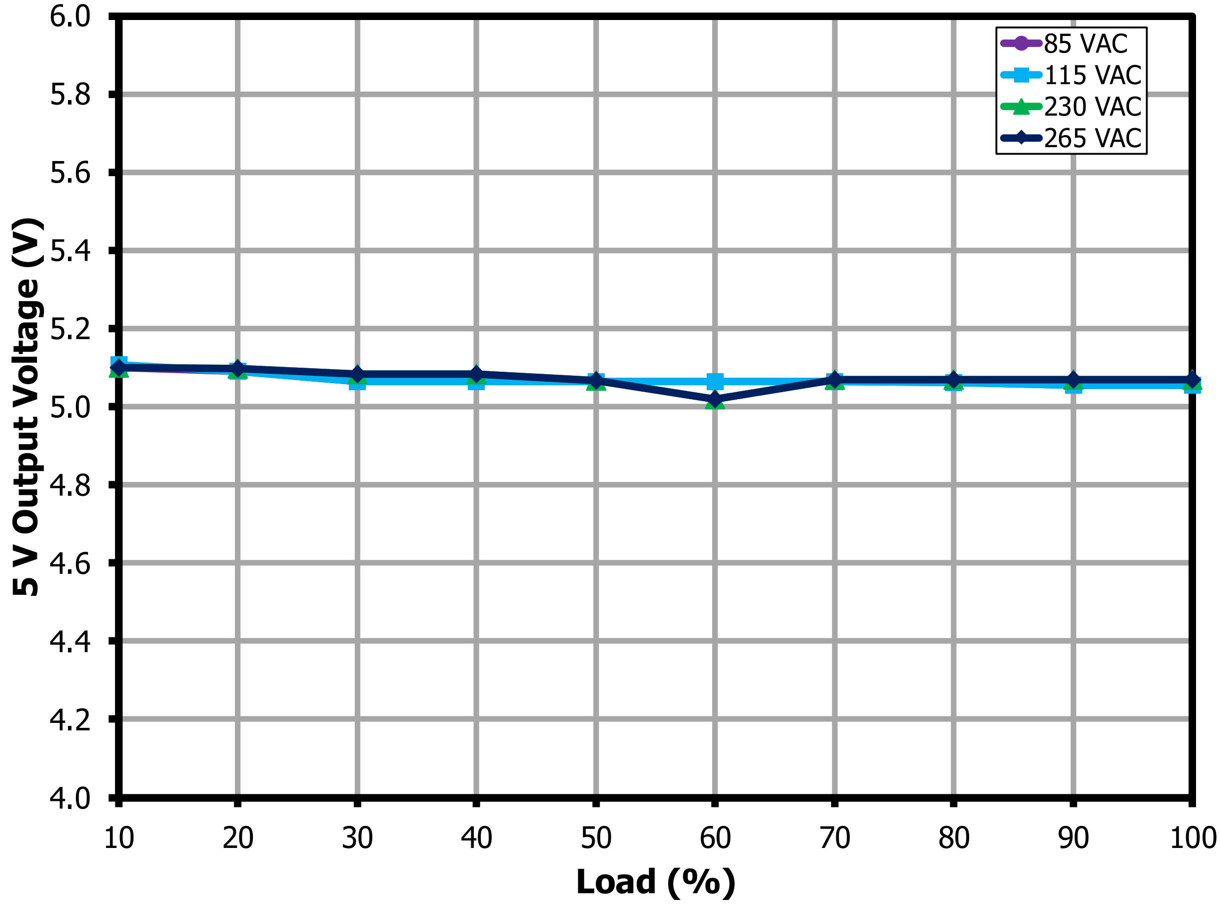

Figure 14 – 5 V Output Voltage vs. Percent Load.

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9.4.1 Load Regulation – 5 V Output is at Minimum Load (5 V / 50 mA)

Test Condition: Soak for 15 minutes each line, and 5 minutes for each load.

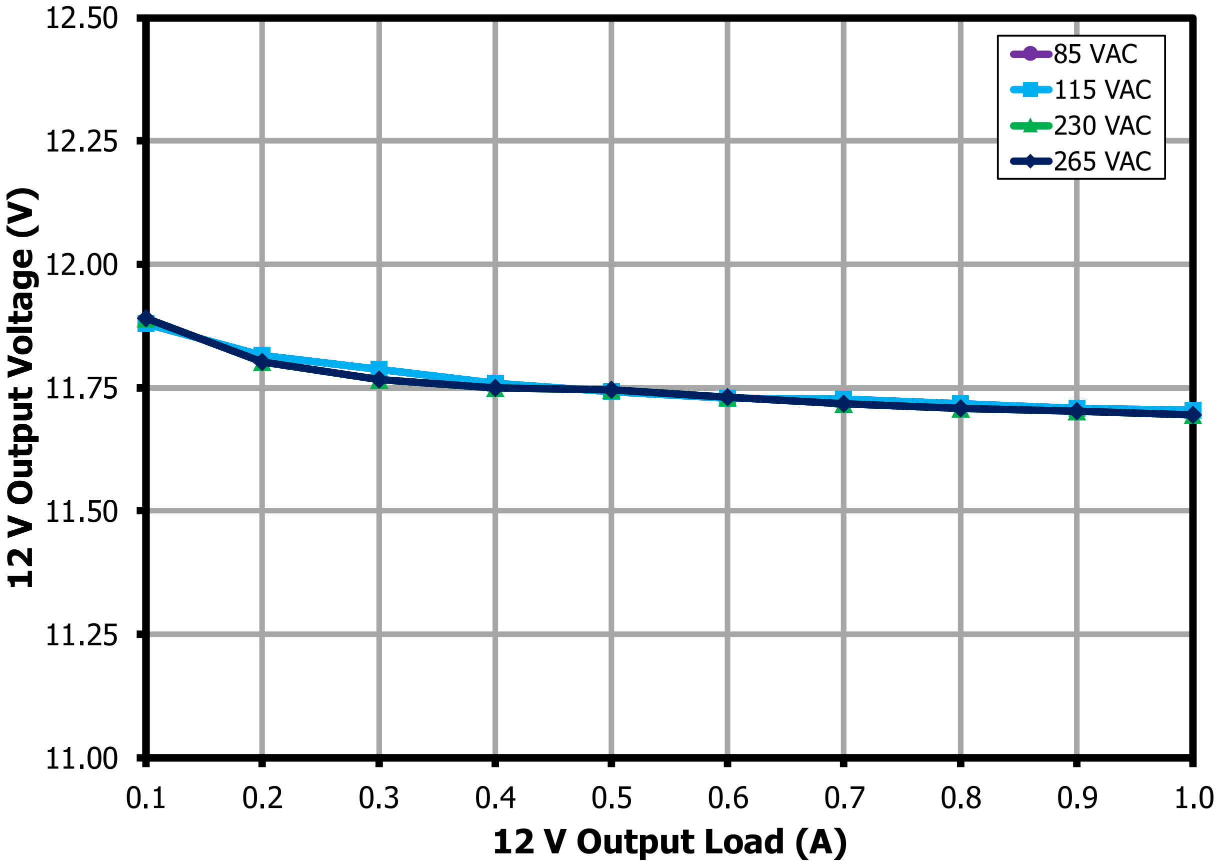

Figure 15 – 12 V Output Voltage vs. 12 V Load Increases.

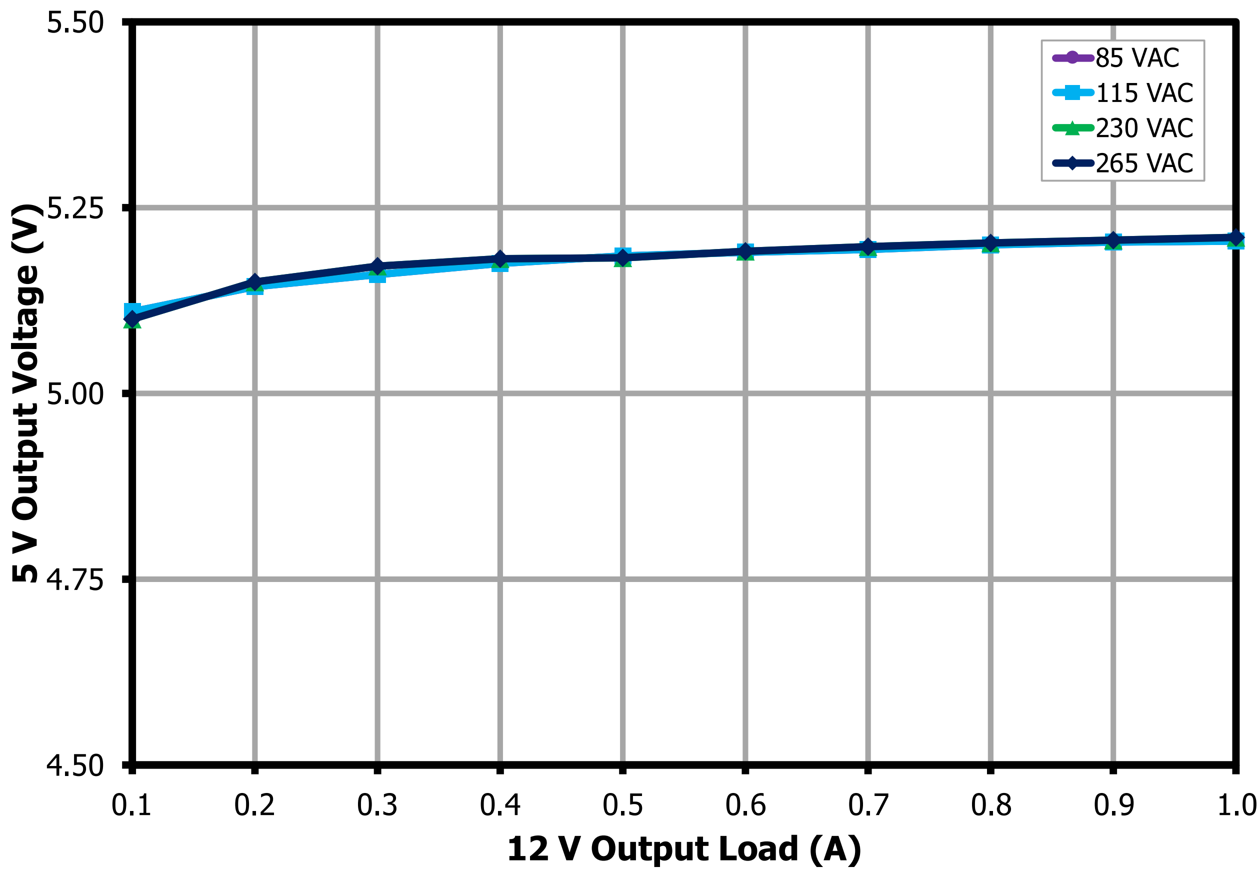

Figure 16 – 5 V Output Voltage vs. 12 V Load Increases.

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9.4.2 Load Regulation – 12 V Output is at Minimum Load (12 V / 0.1 A)

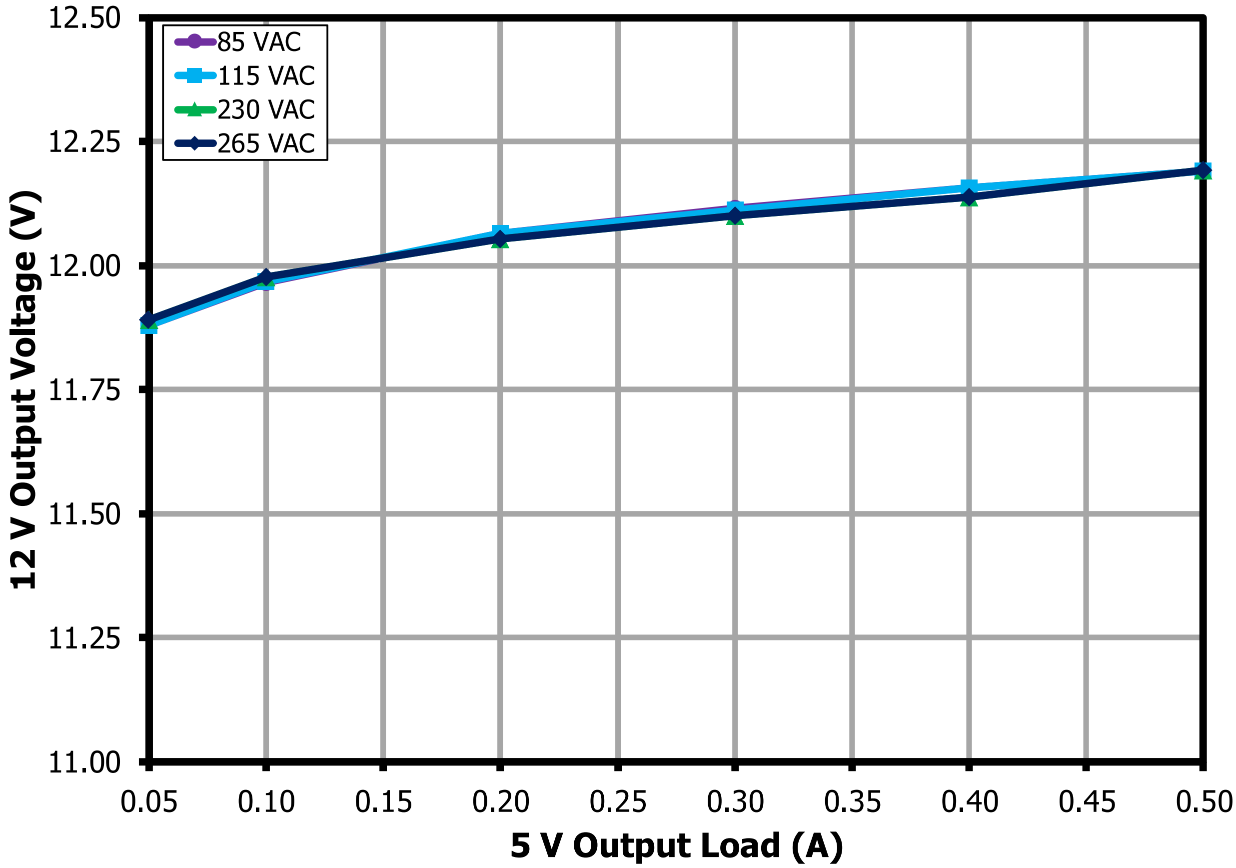

Figure 17 – 12 V Output Voltage vs. 5 V Load Increases.

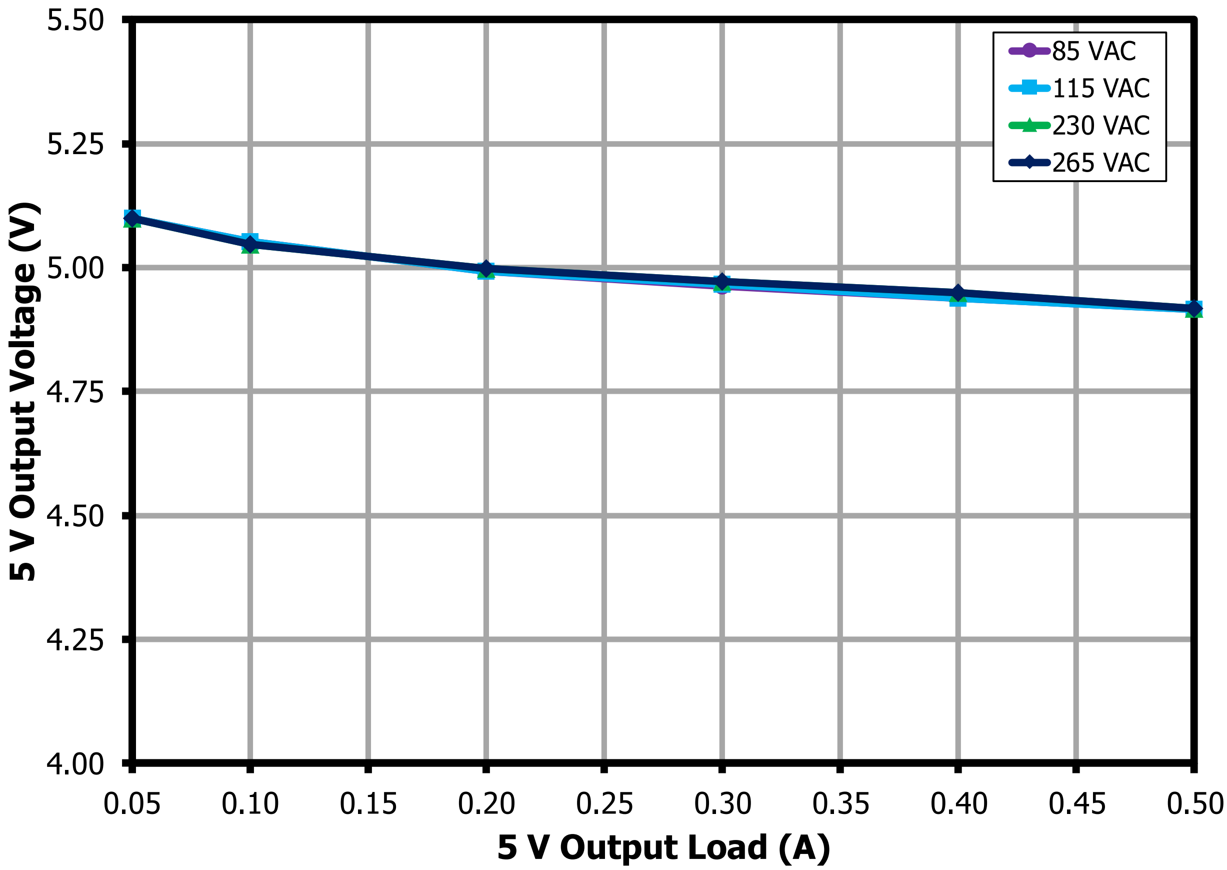

Figure 18 – 5V Output Voltage vs. 5V Load Increases.

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10 Waveforms

10.1 *Load Transient Response*

Test Condition: Dynamic load frequency = 1 kHz, Duty cycle = 50 %

10.1.1 12 V 10% - 100% Load Change / 5 V at 500 mA

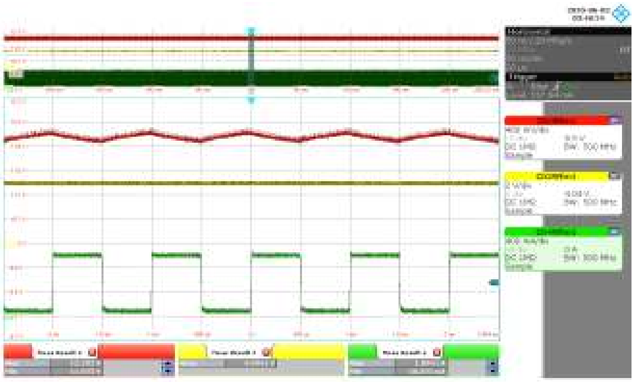

Figure 19 – 85 VAC / 60 Hz.
CH 2: 12 V, 400 mV / div., 50 ms. / div.
CH 3: 5 V, 2 V / div., 50 ms. / div.
CH 4: I_{OUT}, 400 mA / div., 50 ms. / div.
Zoom = 500 µs / div.
V_{MAX} = 12.202 V, V_{MIN} = 11.993 V.

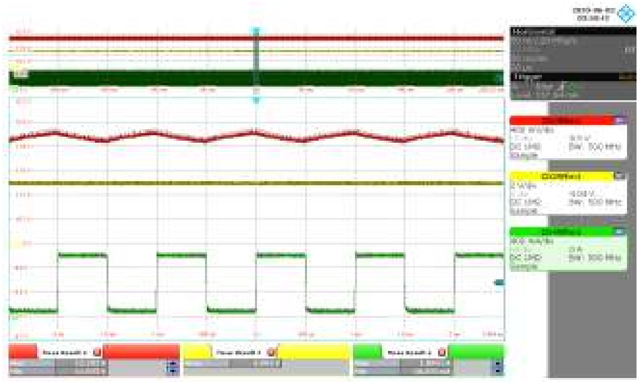

Figure 20 – 115 VAC / 60 Hz.
CH 2: 12 V, 400 mV / div., 50 ms. / div.
CH 3: 5 V, 2 V / div., 50 ms. / div.
CH 4: I_{OUT}, 400 mA / div., 50 ms. / div.
Zoom = 500 µs / div.
V_{MAX} = 12.202 V, V_{MIN} = 11.993 V.

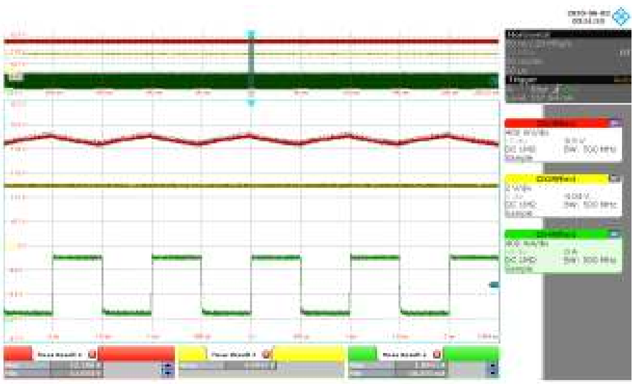

Figure 21 – 230 VAC / 50 Hz.
CH 2: 12 V, 400 mV / div., 50 ms. / div.
CH 3: 5 V, 2 V / div., 50 ms. / div.
CH 4: I_{OUT}, 400 mA / div., 50 ms. / div.
Zoom = 500 µs / div.
V_{MAX} = 12.186 V, V_{MIN} = 11.933 V.

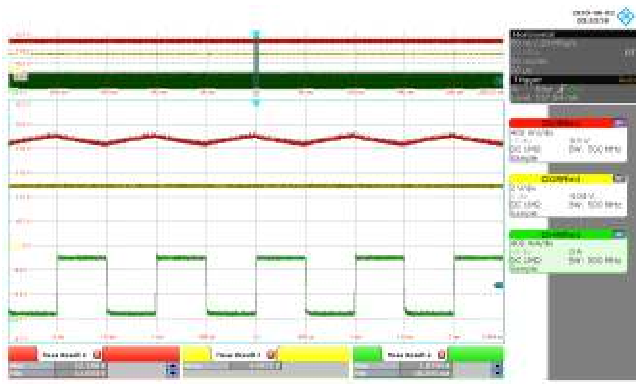

Figure 22 – 265 VAC / 50 Hz.
CH 2: 12 V, 400 mV / div., 50 ms. / div.
CH 3: 5 V, 2 V / div., 50 ms. / div.
CH 4: I_{OUT}, 400 mA / div., 50 ms. / div.
Zoom = 500 µs / div.
V_{MAX} = 12.186 V, V_{MIN} = 11.933 V.

10.1.2 12 V 10% - 100% Load Change / 5 V at 50 mA

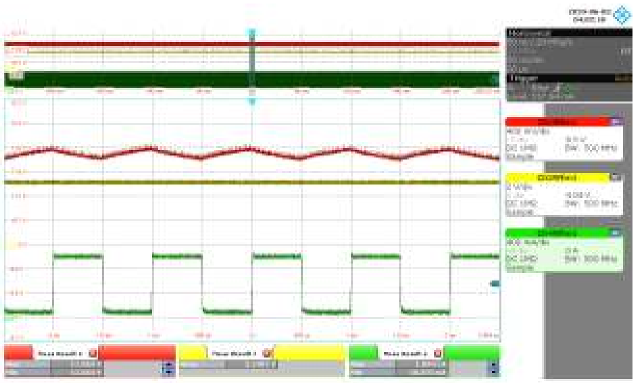

Figure 23 – 85 VAC / 60 Hz.
CH 2: 12 V, 400 mV / div., 50 ms. / div.
CH 3: 5V, 2 V / div., 50 ms. / div.
CH 4: I_{OUT}, 400 mA / div., 50 ms. / div.
Zoom = 500 µs / div.
V_{MAX} = 11.965 V, V_{MIN} = 11.664 V.

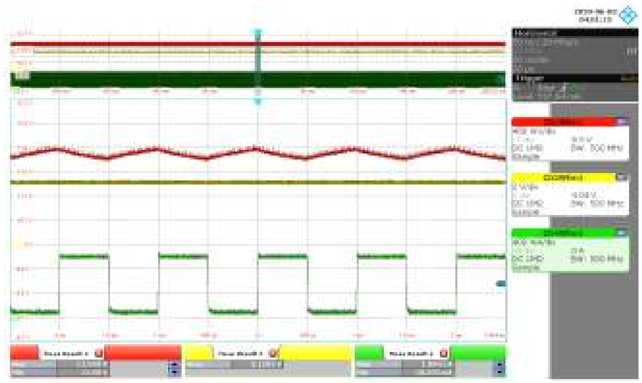

Figure 24 – 115 VAC / 60 Hz.
CH 2: 12 V, 400 mV / div., 50 ms. / div.
CH 3: 5V, 2 V / div., 50 ms. / div.
CH 4: I_{OUT}, 400 mA / div., 50 ms. / div.
Zoom = 500 µs / div.
V_{MAX} = 11.949 V, V_{MIN} = 11.68 V.

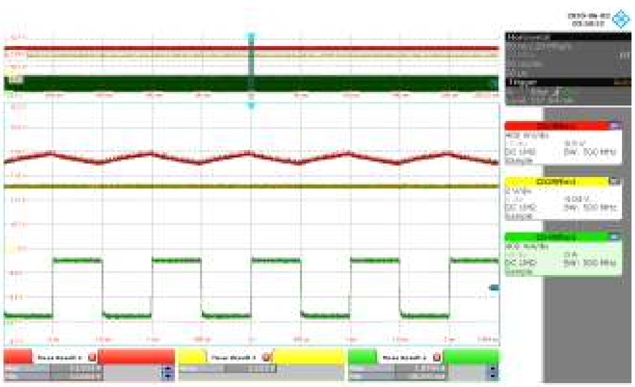

Figure 25 – 230 VAC / 50 Hz.
CH 2: 12 V, 400 mV / div., 50 ms. / div.
CH 3: 5V, 2 V / div., 50 ms. / div.
CH 4: I_{OUT}, 400 mA / div., 50 ms. / div.
Zoom = 500 µs / div.
V_{MAX} = 11.933 V, V_{MIN} = 11.664 V.

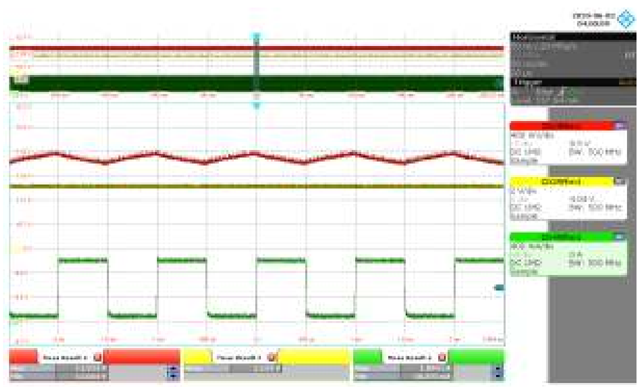

Figure 26 – 265 VAC / 50 Hz.
CH 2: 12 V, 400 mV / div., 50 ms. / div.
CH 3: 5V, 2 V / div., 50 ms. / div.
CH 4: I_{OUT}, 400 mA / div., 50 ms. / div.
Zoom = 500 µs / div.
V_{MAX} = 11.933 V, V_{MIN} = 11.664 V.

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10.1.3 5 V 10% - 100% Load Change / 12 V at 1 A

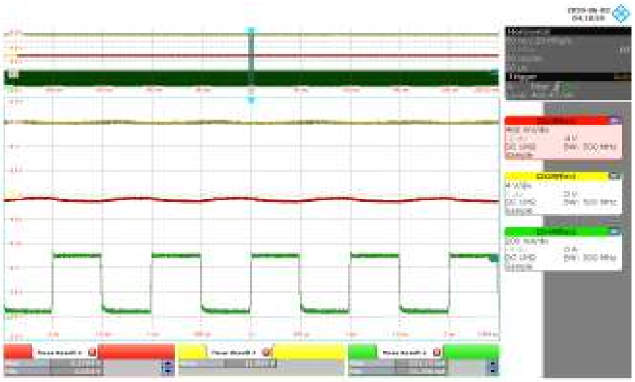

Figure 27 – 85 VAC / 60 Hz.
CH 2: 5 V, 400 mV / div., 50 ms. / div.
CH 3: 12 V, 4 V / div., 50 ms. / div.
CH 4: I_{OUT}, 200 mA / div., 50 ms. / div.
Zoom = 500 µs / div.
V_{MAX} = 5.1794 V, V_{MIN} = 5.053 V.

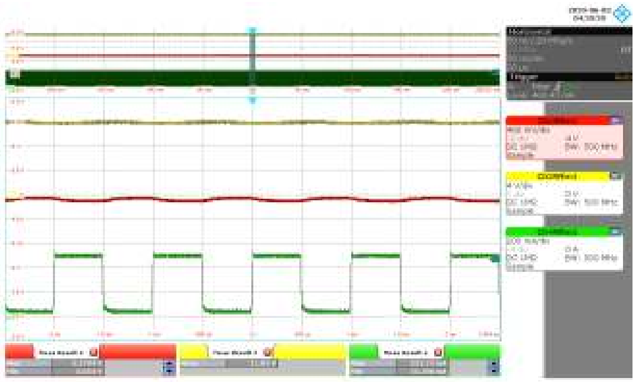

Figure 28 – 115 VAC / 60 Hz.
CH 2: 5 V, 400 mV / div., 50 ms. / div.
CH 3: 12 V, 4 V / div., 50 ms. / div.
CH 4: I_{OUT}, 200 mA / div., 50 ms. / div.
Zoom = 500 µs / div.
V_{MAX} = 5.1794 V, V_{MIN} = 5.053 V.

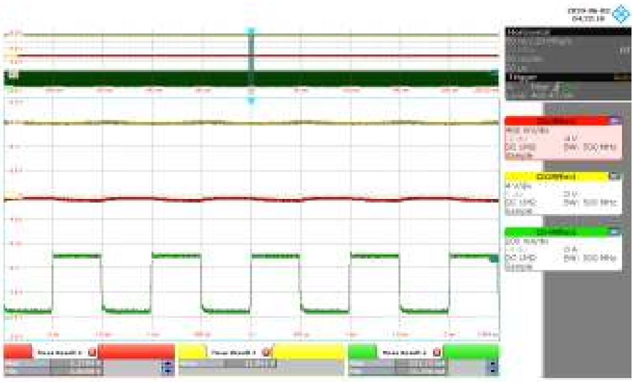

Figure 29 – 230 VAC / 50 Hz.
CH 2: 5 V, 400 mV / div., 50 ms. / div.
CH 3: 12 V, 4 V / div., 50 ms. / div.
CH 4: I_{OUT}, 200 mA / div., 50 ms. / div
Zoom = 500 µs / div.
V_{MAX} = 5.1794 V, V_{MIN} = 5.0688 V.

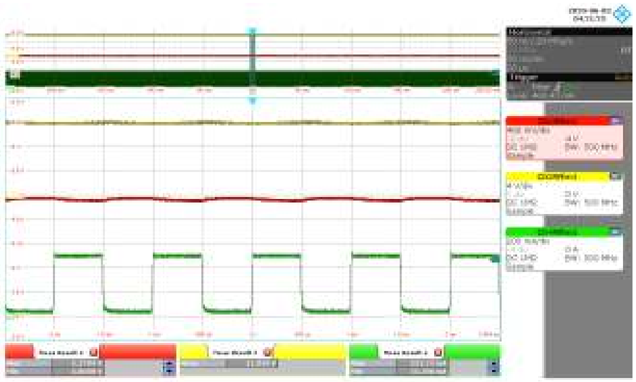

Figure 30 – 265 VAC / 50 Hz.
CH 2: 5 V, 400 mV / div., 50 ms. / div.
CH 3: 12 V, 4 V / div., 50 ms. / div.
CH 4: I_{OUT}, 200 mA / div., 50 ms. / div.
Zoom = 500 µs / div.
V_{MAX} = 5.1794 V, V_{MIN} = 5.0688 V.

10.2 *Output Voltage at Start-up*

10.2.1 CC Mode

10.2.1.1 100% Load

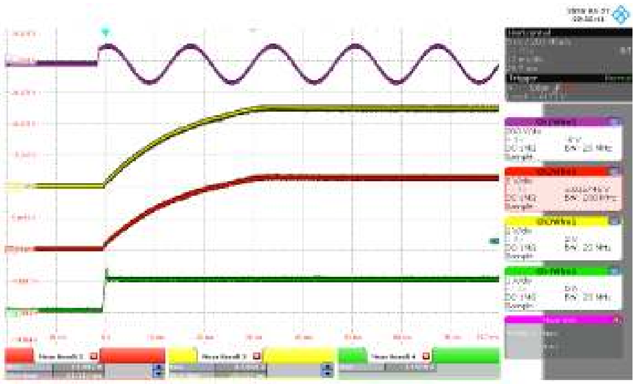

Figure 31 – 85 VAC / 60 Hz 100% Load.
CH 1: V_{IN}, 200 V / div., 10 ms. / div.
CH 2: 12 V, 5 V / div., 10 ms. / div.
CH 3: 5 V, 2 V / div., 10 ms. / div.
CH 4: I_{OUT} (12 V), 1 A / div., 10 ms. / div.
12 V Rise Time: 21.117 ms.
5 V Rise Time: 20.817 ms.

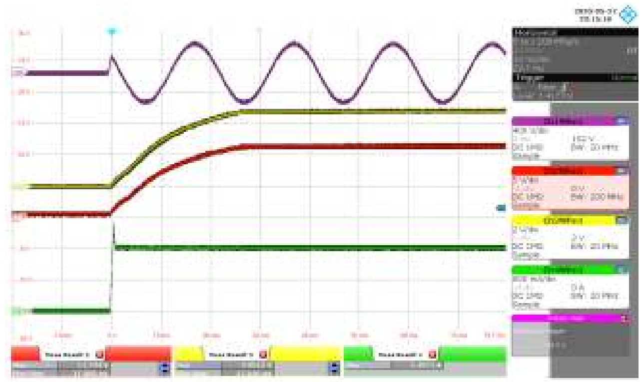

Figure 32 – 265 VAC / 60 Hz 100% Load.
CH 1: V_{IN}, 400 V / div., 10 ms. / div.
CH 2: 12 V, 5 V / div., 10 ms. / div.
CH 3: 5 V, 2 V / div., 10 ms. / div.
CH 4: I_{OUT} (12 V), 500 mA / div., 10 ms. / div.
12 V Rise Time: 17.808 ms.
5 V Rise Time: 17.046 ms.

10.2.1.2 10% Load

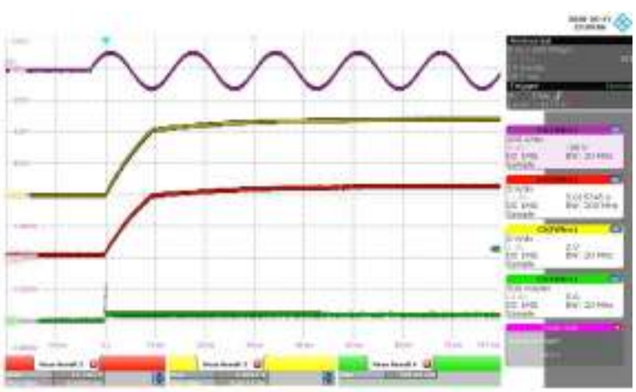

Figure 33 – 85 VAC / 60 Hz 10% Load.
CH 1: V_{IN}, 200 V / div., 10 ms. / div.
CH 2: 12 V, 5 V / div., 10 ms. / div.
CH 3: 5 V, 2 V / div., 10 ms. / div.
CH 4: I_{OUT} (12 V), 500 mA / div., 10 ms. / div.
12 V Rise Time: 8.509 ms.
5 V Rise Time: 9.608 ms.

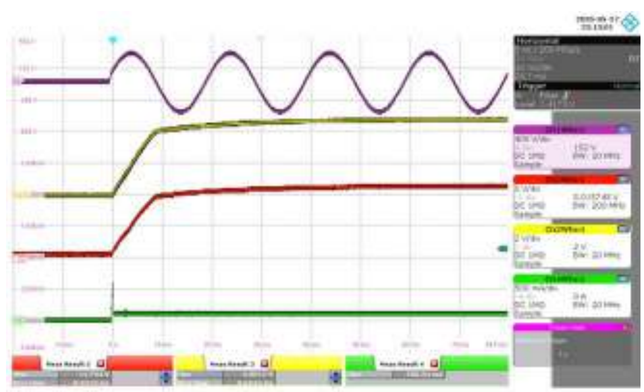

Figure 34 – 265 VAC / 60 Hz 10% Load.
CH 1: V_{IN}, 400 V / div., 10 ms. / div.
CH 2: 12 V, 5 V / div., 10 ms. / div.
CH 3: 5 V, 2 V / div., 10 ms. / div.
CH 4: I_{OUT} (12 V), 500 mA / div., 10 ms. / div.
12 V Rise Time: 8.852 ms.
5 V Rise Time: 9.695 ms.

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10.3 *Switching Waveforms*

10.3.1 Primary MOSFET Drain-Source Voltage and Current at Normal Operation

10.3.1.1 100% Load

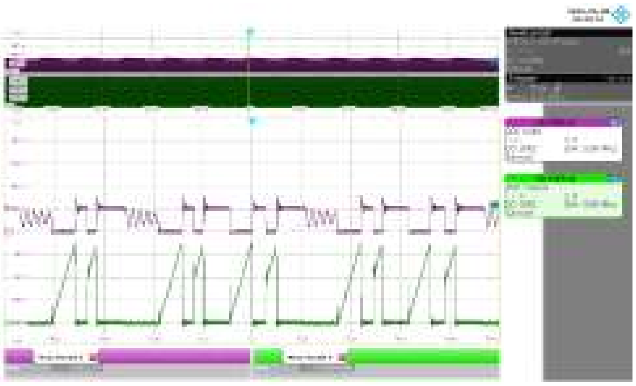

Figure 35 – 85 VAC / 60 Hz 100% Load.
CH 1: V_{DS}, 200 V / div., 10 ms. / div.
CH 4: I_{DS}, 200 mA / div., 10 ms. / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$: 316.21 V, $I_{DS(MAX)}$: 713.04 mA.

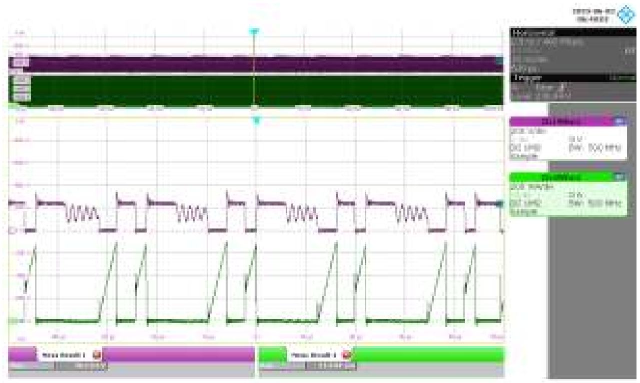

Figure 36 – 115 VAC / 60 Hz 100% Load.
CH 1: V_{DS}, 200 V / div., 10 ms. / div.
CH 4: I_{DS}, 200 mA / div., 10 ms. / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$: 363.64 V, $I_{DS(MAX)}$: 713.04 mA.

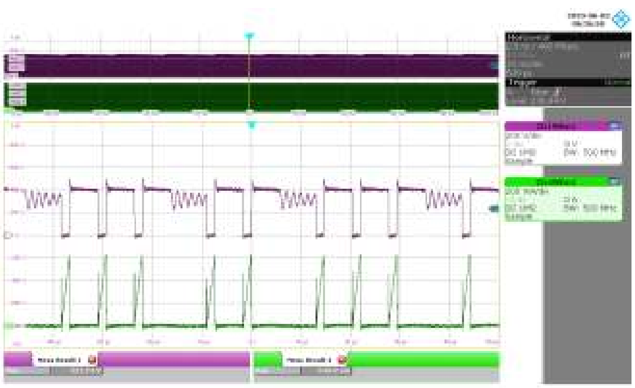

Figure 37 – 230 VAC / 60 Hz 100% Load.
CH 1: V_{DS}, 200 V / div., 10 ms. / div.
CH 4: I_{DS}, 200 mA / div., 10 ms. / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$: 521.74 V, $I_{DS(MAX)}$: 649.8 mA.

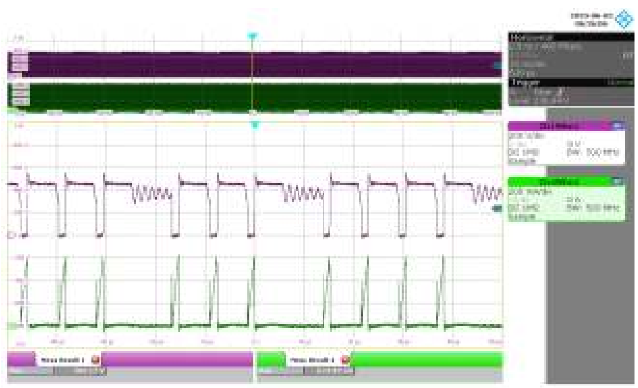

Figure 38 – 265 VAC / 60 Hz 100% Load.
CH 1: V_{DS}, 200 V / div., 10 ms. / div.
CH 4: I_{DS}, 200 mA / div., 10 ms. / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$: 569.17 V, $I_{DS(MAX)}$: 633.99 mA.

10.3.1.2 10% Load

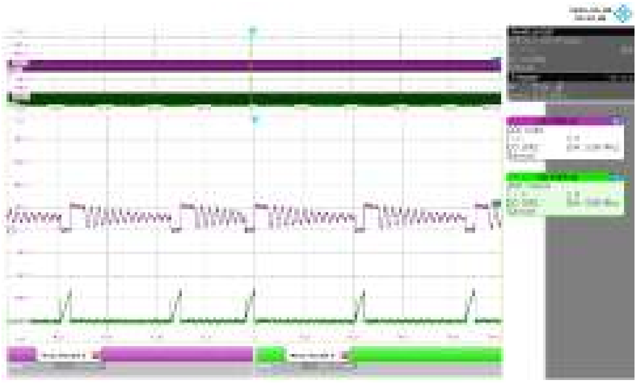

Figure 39 – 85 VAC / 60 Hz 10% Load.
CH 1: V_{DS}, 200 V / div., 10 ms. / div.
CH 4: I_{DS}, 200 mA / div., 10 ms. / div.
Zoom: 10 μs / div.
$V_{DS(MAX)}$: 252.96 V, $I_{DS(MAX)}$: 286.17 mA .

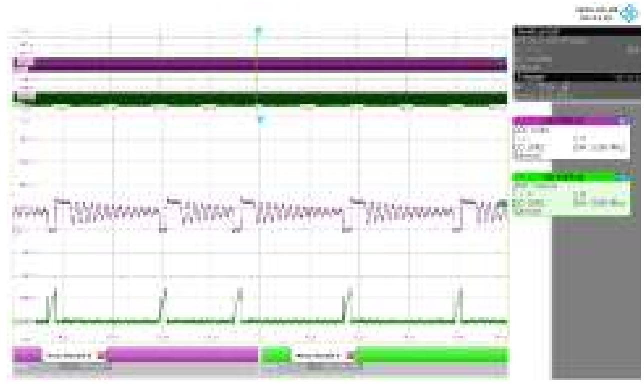

Figure 40 – 115 VAC / 60 Hz 10% Load.
CH 1: V_{DS}, 200 V / div., 10 ms. / div.
CH 4: I_{DS}, 200 mA / div., 10 ms. / div.
Zoom: 10 μs / div.
$V_{DS(MAX)}$: 292.49 V, $I_{DS(MAX)}$: 301.98 mA.

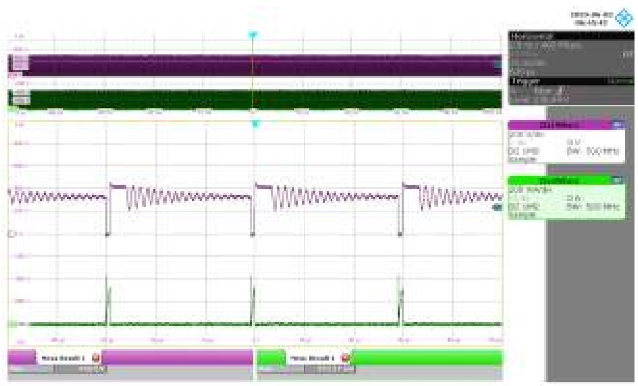

Figure 41 – 230 VAC / 50 Hz 10% Load.
CH 1: V_{DS}, 200 V / div., 10 ms. / div
CH 4: I_{DS}, 200 mA / div., 10 ms. / div.
Zoom: 10 μs / div.
$V_{DS(MAX)}$: 458.5 V, $I_{DS(MAX)}$: 452.17 mA.

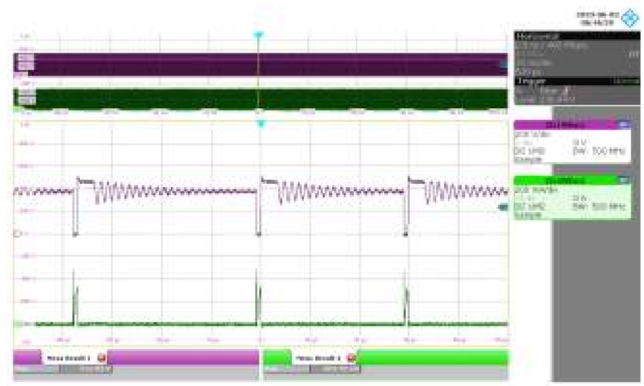

Figure 42 – 265 VAC / 50 Hz 10% Load.
CH 1: V_{DS}, 200 V / div., 10 ms. / div.
CH 4: I_{DS}, 200 mA / div., 10 ms. / div.
Zoom: 10 μs / div.
$V_{DS(MAX)}$: 513.63 V, $I_{DS(MAX)}$: 483.79 mA.

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10.3.2 Primary MOSFET Drain-Source Voltage and Current at Start-up Operation

10.3.2.1 100% Load

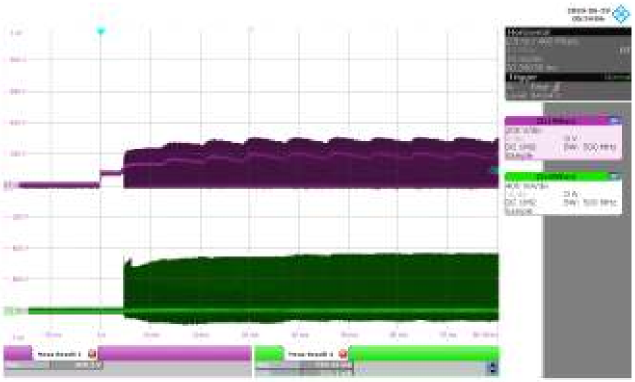

Figure 43 – 85 VAC / 60 Hz 100% Load.
CH 1: V_{DS}, 200 V / div., 10 ms. / div.
CH 4: I_{DS}, 400 mA / div., 10 ms. / div.
$V_{DS(MAX)}$: 308.3 V, $I_{DS(MAX)}$: 730.43 mA.

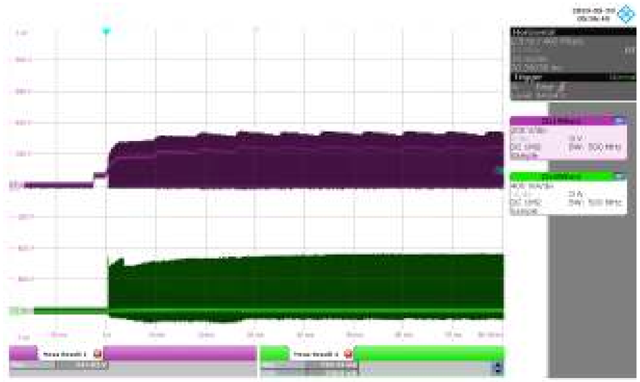

Figure 44 – 115 VAC / 60 Hz 100% Load
CH 1: V_{DS}, 200 V / div., 10 ms. / div.
CH 4: I_{DS}, 400 mA / div., 10 ms. / div.
$V_{DS(MAX)}$: 347.83 V, $I_{DS(MAX)}$: 730.43 mA.

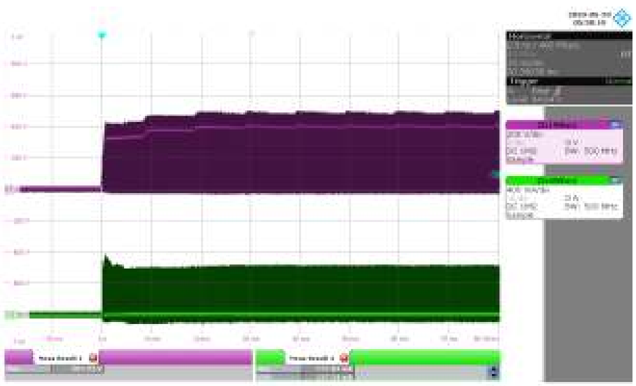

Figure 45 – 230 VAC / 50 Hz 100% Load.
CH 1: V_{DS}, 200 V / div., 10 ms. / div
CH 4: I_{DS}, 400 mA / div., 10 ms. / div.
$V_{DS(MAX)}$: 505.93 V, $I_{DS(MAX)}$: 777.87 mA.

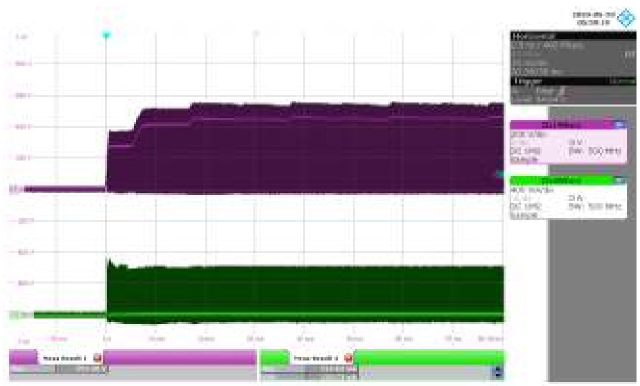

Figure 46 – 265 VAC / 50 Hz 100% Load.
CH 1: V_{DS}, 200 V / div., 10 ms. / div.
CH 4: I_{DS}, 400 mA / div., 10 ms. / div.
$V_{DS(MAX)}$: 553.36 V, $I_{DS(MAX)}$: 714.62 mA.

10.3.3 Output Diode Voltage and Current at Normal Operation

10.3.3.1 100% Load – 12 V Output Diode (D3)

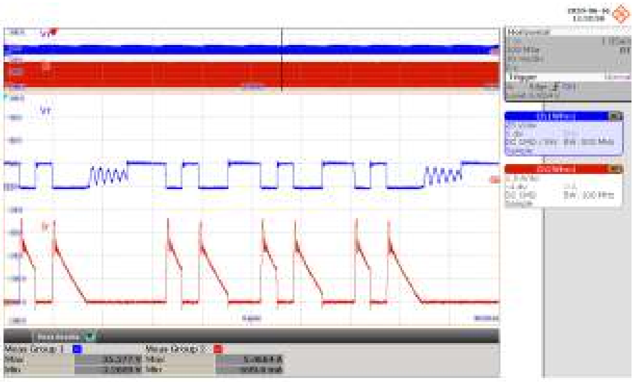

Figure 47 – 85 VAC / 60 Hz 100% Load.
CH 1: V_{R_D3}, 25 V / div., 10 ms. / div.
CH 4: I_{D3}, 1.5 A / div., 10 ms. / div.
Zoom: 8 μs / div.
PIV: 35.277 V, $I_{D(MAX)}$: 5.4664 A.

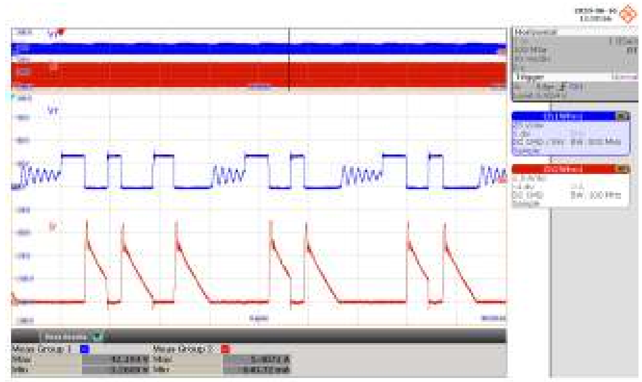

Figure 48 – 115 VAC / 60 Hz 100% Load.
CH 1: V_{R_D3}, 25 V / div., 10 ms. / div.
CH 4: I_{D3}, 1.5 A / div., 10 ms. / div.
Zoom: 8 μs / div.
PIV: 42.194 V, $I_{D(MAX)}$: 5.4071 A.

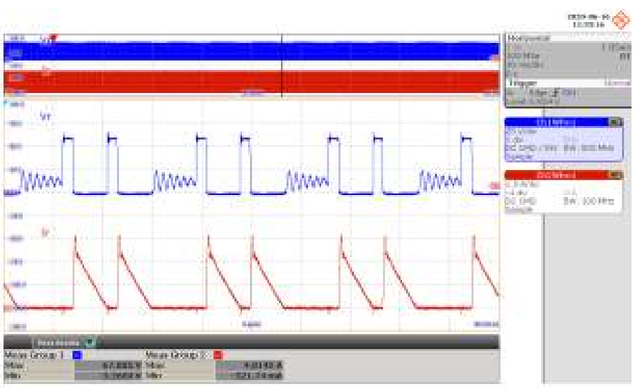

Figure 49 – 230 VAC / 50 Hz 100% Load.
CH 1: V_{R_D3}, 25 V / div., 10 ms. / div.
CH 4: I_{D3}, 1.5 A / div., 10 ms. / div.
Zoom: 8 μs / div.
PIV: 67.885 V, $I_{D(MAX)}$: 4.8142 A.

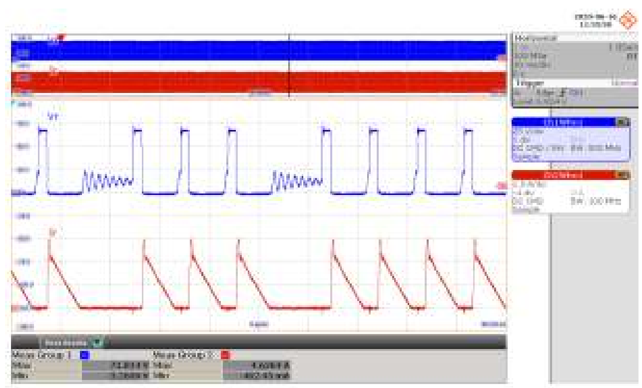

Figure 50 – 265 VAC / 50 Hz 100% Load.
CH 1: V_{R_D3}, 25 V / div., 10 ms. / div.
CH 4: I_{D3}, 1.5 A / div., 10 ms. / div.
Zoom: 8 μs / div.
PIV: 73.814 V, $I_{D(MAX)}$: 4.6364 A.

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10.3.3.2 10% Load – 12 V Output Diode (D3)

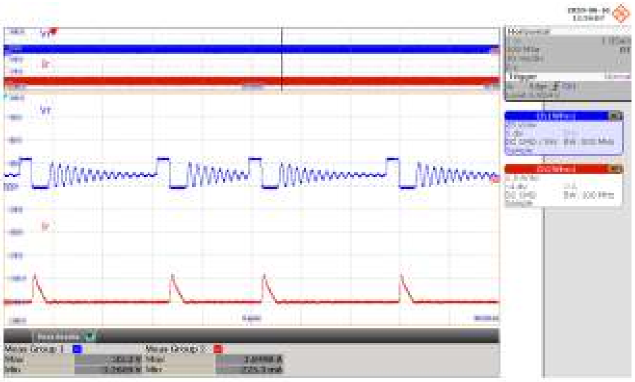

Figure 51 – 85 VAC / 60 Hz 10% Load.
CH 1: V_{R_D3}, 25 V / div., 10 ms. / div.
CH 4: I_{D3}, 1.5 A / div., 10 ms. / div.
Zoom: 8 μs / div.
PIV: 33.3 V, $I_{D(MAX)}$: 1.8498 A.

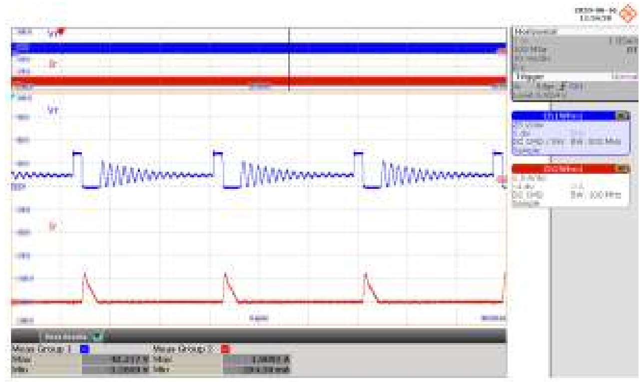

Figure 52 – 115 VAC / 60 Hz 10% Load.
CH 1: V_{R_D3}, 25 V / div., 10 ms. / div.
CH 4: I_{D3}, 1.5 A / div., 10 ms. / div.
Zoom: 8 μs / div.
PIV: 40.217 V, $I_{D(MAX)}$: 1.9091 A.

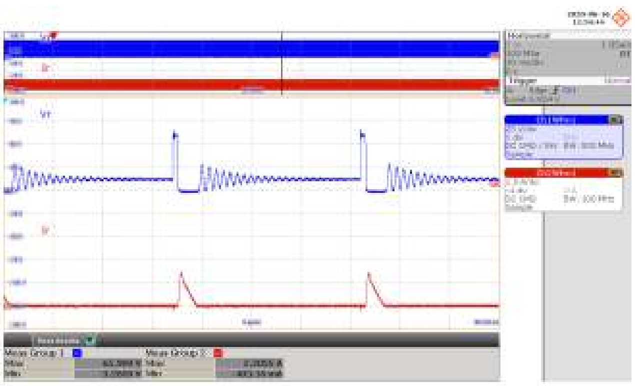

Figure 53 – 230 VAC / 50 Hz 10% Load.
CH 1: V_{R_D3}, 25 V / div., 10 ms. / div.
CH 4: I_{D3}, 1.5 A / div.
Zoom: 10 μs / div.
PIV: 65.909 V, $I_{D(MAX)}$: 2.2055 A.

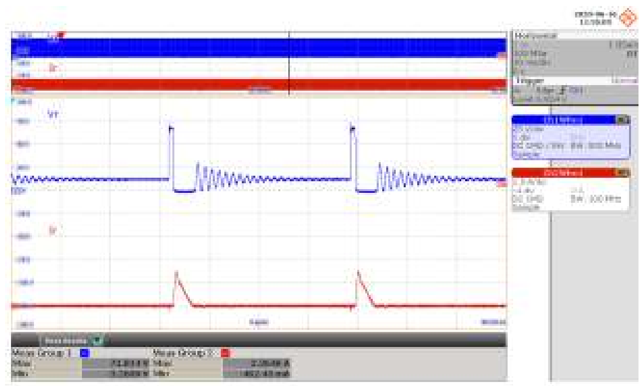

Figure 54 – 265 VAC / 50 Hz 10% Load**.**
CH 1: V_{R_D3}, 25 V / div., 10 ms. / div.
CH 4: I_{D3}, 1.5 A / div.
Zoom: 10 μs / div.
PIV: 73.814 V, $I_{D(MAX)}$: 2.2648 A.

10.3.3.3 100% Load – 5 V Output Diode (D4)

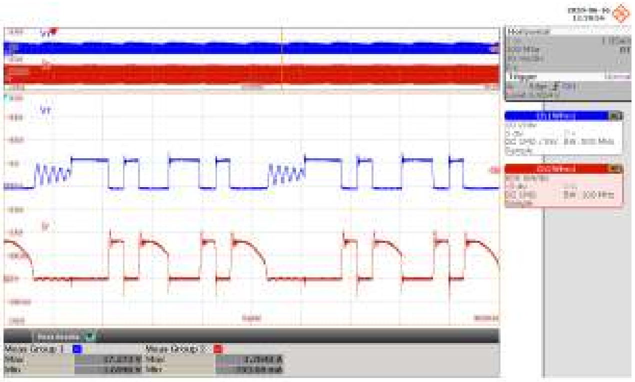

Figure 55 – 85 VAC / 60 Hz 100% Load.
CH 1: V_{R_D4}, 10 V / div., 10 ms. / div.
CH 4: I_{D4}, 800 mA / div., 10 ms. / div.
Zoom: 8 μs / div.
PIV: 17.273 V, $I_{D(MAX)}$: 1.7043 A.

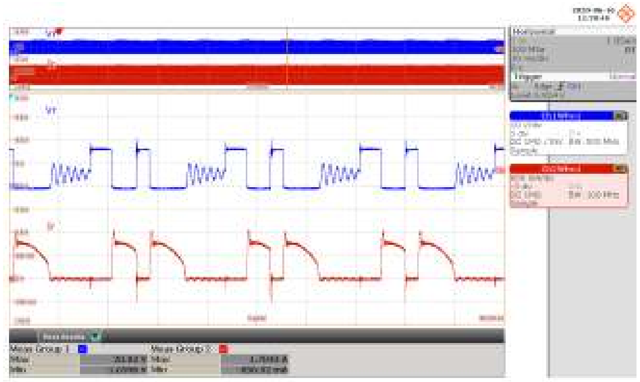

Figure 56 – 115 VAC / 60 Hz 100% Load.
CH 1: V_{R_D4}, 10 V / div., 10 ms. / div.
CH 4: I_{D4}, 800 mA / div., 10 ms. / div.
Zoom: 8 μs / div.
PIV: 20.83 V, $I_{D(MAX)}$: 1.7043 A.

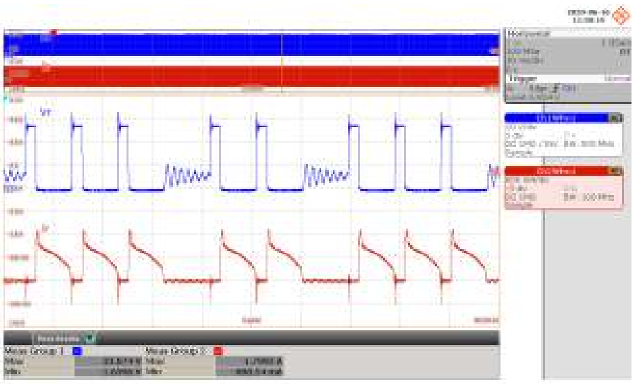

Figure 57 – 230 VAC / 50 Hz 100% Load.
CH 1: V_{R_D4}, 10 V / div., 10 ms. / div.
CH 4: I_{D4}, 800 mA / div., 10 ms. / div.
Zoom: 8 μs / div.
PIV: 33.874 V, $I_{D(MAX)}$: 1.7992 A.

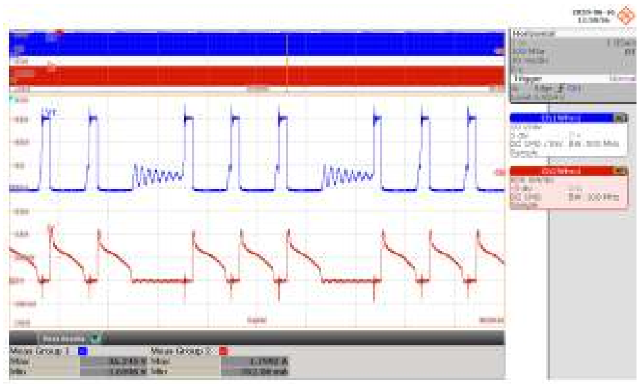

Figure 58 – 265 VAC / 50 Hz 100% Load.
CH 1: V_{R_D4}, 10 V / div., 10 ms. / div.
CH 4: I_{D4}, 800 mA / div., 10 ms. / div.
Zoom: 8 μs / div.
PIV: 36.245 V, $I_{D(MAX)}$: 1.7992 A.

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10.3.3.4 10% Load – 5 V Output Diode (D4)

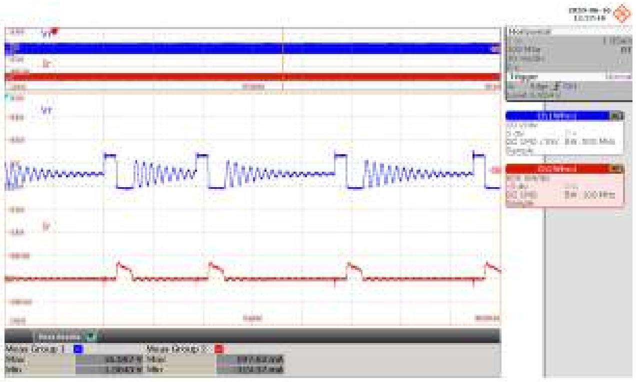

Figure 59 – 85 VAC / 60 Hz 10% Load.
CH 1: V_{R_D4}, 10 V / div., 10 ms. / div.
CH 4: I_{D4}, 800 mA / div., 10 ms. / div.
Zoom: 8 µs / div.
PIV: 16.087 V, $I_{D(MAX)}$: 597.63 mA.

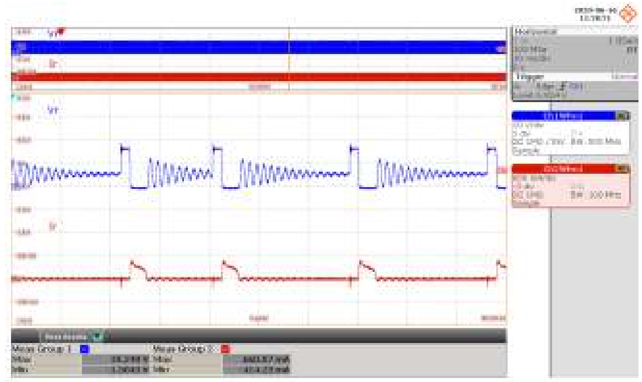

Figure 60 – 115 VAC / 60 Hz 10% Load.
CH 1: V_{R_D4}, 10 V / div., 10 ms. / div.
CH 4: I_{D4}, 800 mA / div., 10 ms. / div.
Zoom: 8 µs / div.
PIV: 19.249 V, $I_{D(MAX)}$: 660.87 mA

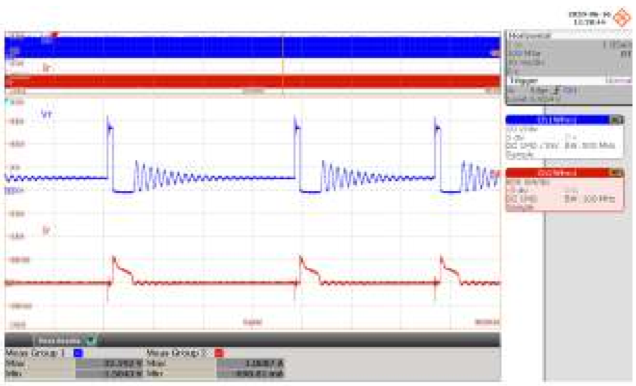

Figure 61 – 230 VAC / 50 Hz 10% Load.
CH 1: V_{R_D4}, 10 V / div., 10 ms. / div.
CH 4: I_{D4}, 800 mA / div., 10 ms. / div.
Zoom: 8 µs / div.
PIV: 32.292 V, $I_{D(MAX)}$: 1.0087 A.

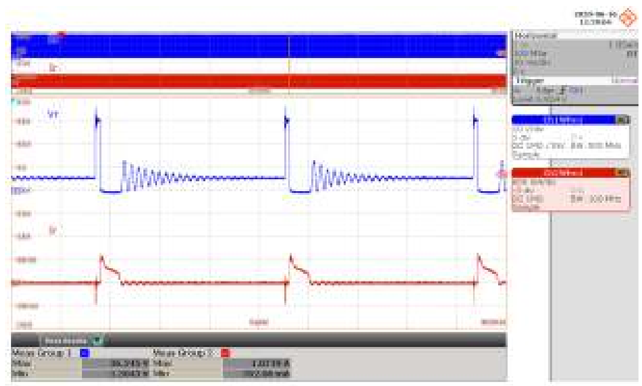

Figure 62 – 265 VAC / 50 Hz 10% Load.
CH 1: V_{R_D4}, 10 V / div., 10 ms. / div.
CH 4: I_{D4}, 800 mA / div., 10 ms. / div..
Zoom: 8 µs / div.
PIV: 36.245 V, $I_{D(MAX)}$: 1.0719 A.

10.3.4 Output Diode Voltage and Current at Start-up Operation

10.3.4.1 100% Load – 12 V Output Diode (D3)

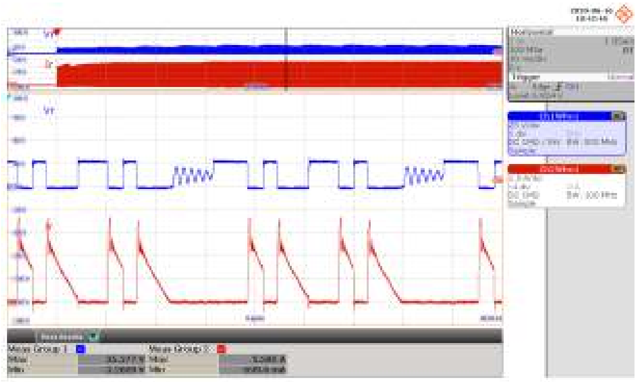

Figure 63 – 85 VAC / 60 Hz 100% Load.
CH 1: V_{R_D3}, 25 V / div., 10 ms. / div.
CH 4: I_{D3}, 1.5 A / div., 10 ms. / div.
Zoom: 8 µs / div.
PIV: 35.277 V, $I_{D(MAX)}$: 5.585 A.

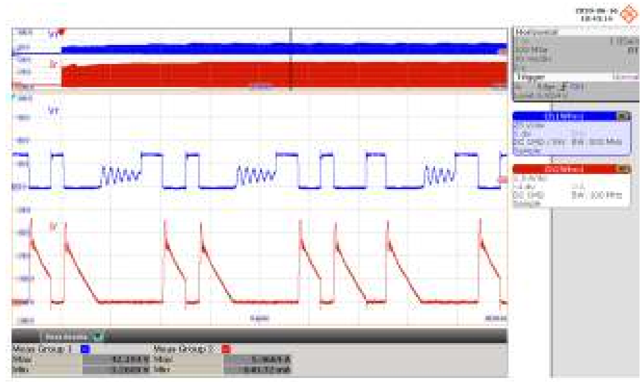

Figure 64 – 115 VAC / 60 Hz 100% Load.
CH 1: V_{R_D3}, 25 V / div., 10 ms. / div.
CH 4: I_{D3}, 1.5 A / div., 10 ms. / div..
Zoom: 8 µs / div.
PIV: 42.194 V, $I_{D(MAX)}$: 5.4644 A.

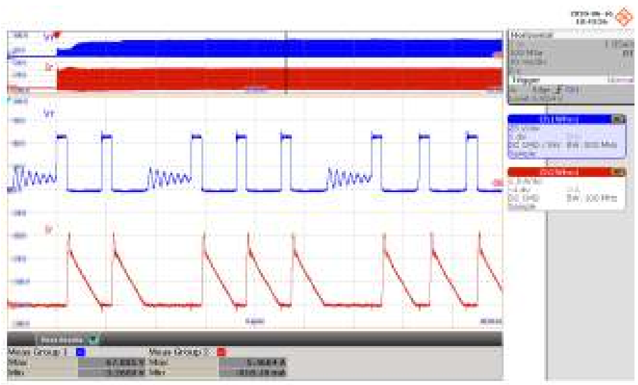

Figure 65 – 230 VAC / 50 Hz 100% Load.
CH 1: V_{R_D3}, 25 V / div., 10 ms. / div
CH 4: I_{D3}, 1.5 A / div., 10 ms. / div.
Zoom: 8 µs / div.
PIV: 67.885 V, $I_{D(MAX)}$: 5.4664 A.

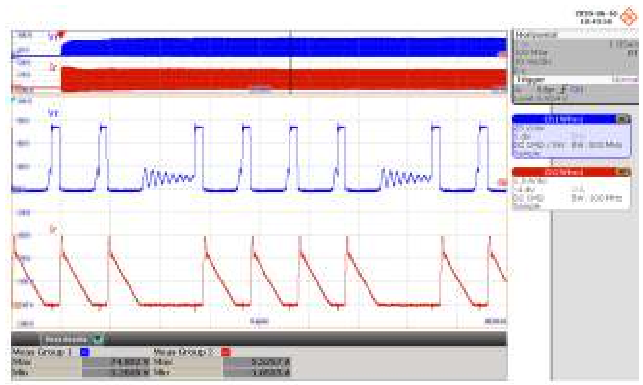

Figure 66 – 265 VAC / 50 Hz 100% Load.
CH 1: V_{R_D3}, 25 V / div., 10 ms. / div.
CH 4: I_{D3}, 1.5 A / div., 10 ms. / div.
Zoom: 8 µs / div.
PIV: 74.802 V, $I_{D(MAX)}$: 5.5257 A.

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10.3.4.2 10% Load – 12 V Output Diode (D3)

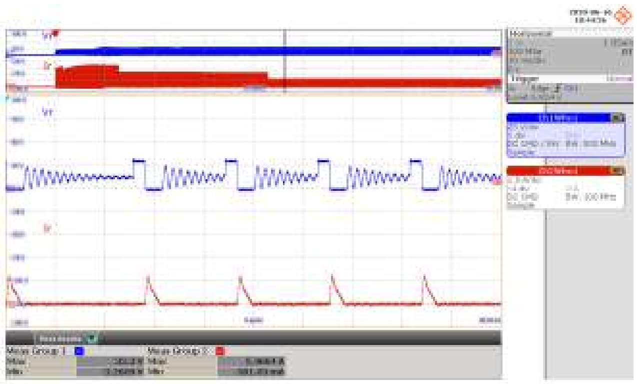

Figure 67 – 85 VAC / 60 Hz 10% Load.
CH 1: V_{R_D3}, 25 V / div., 10 ms. / div.
CH 4: I_{D3}, 1.5 A / div., 10 ms. / div.
Zoom: 8 μs / div.
PIV: 33.3 V, $I_{D(MAX)}$: 5.4664 A.

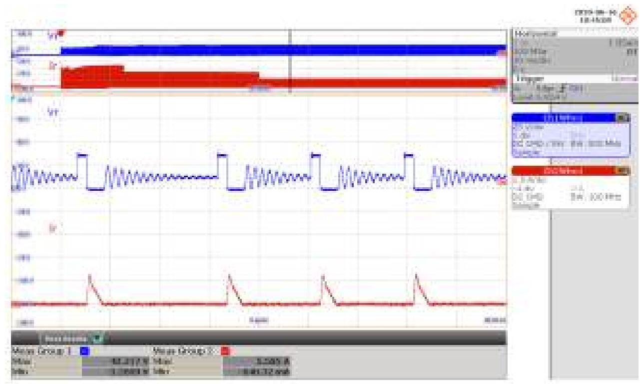

Figure 68 – 115 VAC / 60 Hz 10% Load.
CH 1: V_{R_D3}, 25 V / div., 10 ms. / div.
CH 4: I_{D3}, 1.5 A / div., 10 ms. / div.
Zoom: 8 μs / div.
PIV: 40.217 V, $I_{D(MAX)}$: 5.585 A.

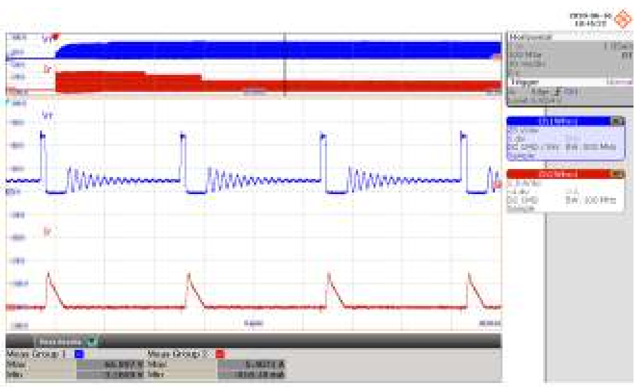

Figure 69 – 230 VAC / 50 Hz 10% Load.
CH 1: V_{R_D3}, 25 V / div., 10 ms. / div.
CH 4: I_{D3}, 1.5 A / div., 10 ms. / div.
Zoom: 8 μs / div.
PIV: 66.897 V, $I_{D(MAX)}$: 5.4071 A.

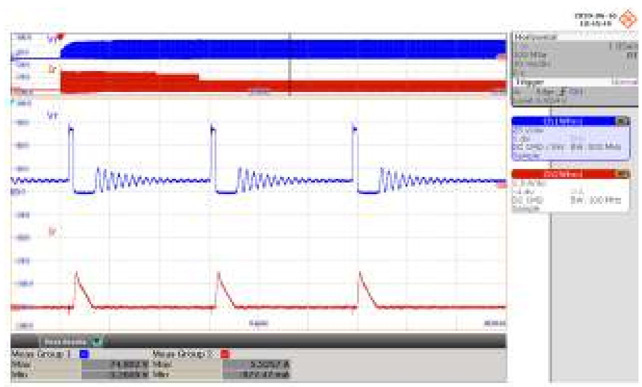

Figure 70 – 265 VAC / 50 Hz 10% Load.
CH 1: V_{R_D3}, 25 V / div., 10 ms. / div.
CH 4: I_{D3}, 1.5 A / div., 10 ms. / div.
Zoom: 8 μs / div.
PIV: 74.802 V, $I_{D(MAX)}$: 5.5257 A.

10.3.4.3 100% Load – 5 V Output Diode (D4)

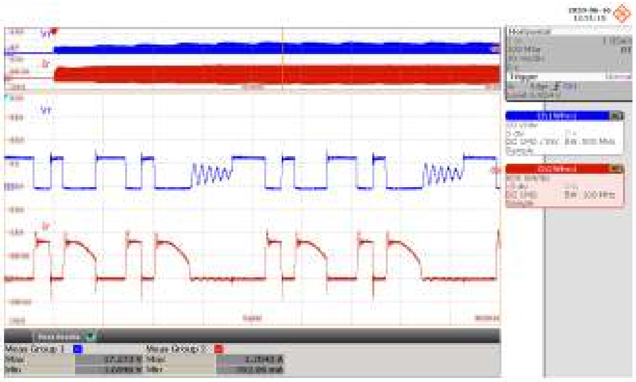

Figure 71 – 85 VAC / 60 Hz 100% Load.
CH 1: V_{R_D4}, 10 V / div., 10 ms. / div.
CH 4: I_{D4}, 800 mA / div., 10 ms. / div.
Zoom: 8 µs / div.
PIV: 17.273 V, $I_{D(MAX)}$: 1.7043 A.

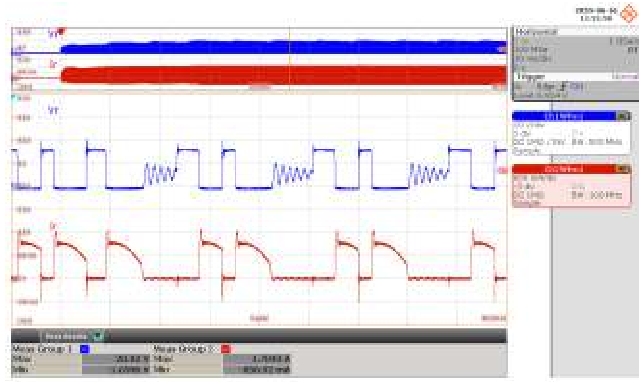

Figure 72 – 115 VAC / 60 Hz 100% Load.
CH 1: V_{R_D4}, 10 V / div., 10 ms. / div.
CH 4: I_{D4}, 800 mA / div., 10 ms. / div.
Zoom: 8 µs / div.
PIV: 20.83 V, $I_{D(MAX)}$: 1.7043 A.

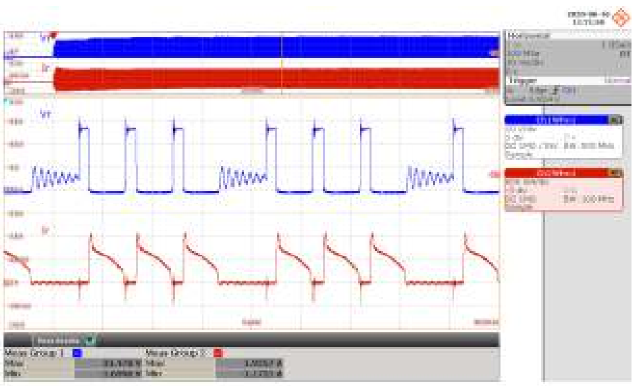

Figure 73 – 230 VAC / 50 Hz 100% Load.
CH 1: V_{R_D4}, 10 V / div., 10 ms. / div.
CH 4: I_{D4}, 800 mA / div., 10 ms. / div.
Zoom: 8 µs / div.
PIV: 33.478 V, $I_{D(MAX)}$: 1.9257 A.

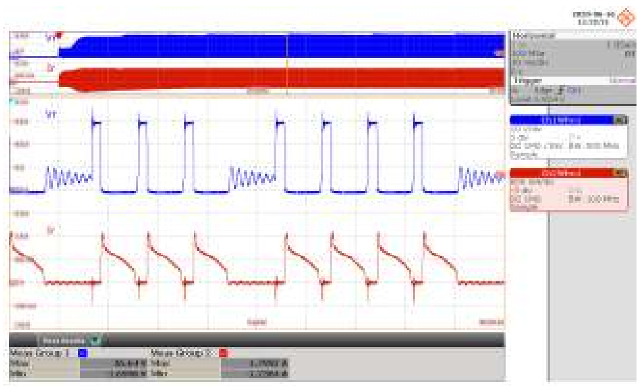

Figure 74 – 265 VAC / 50 Hz 100% Load.
CH 1: V_{R_D4}, 10 V / div., 10 ms. / div.
CH 4: I_{D4}, 800 mA / div., 10 ms. / div.
Zoom: 8 µs / div.
PIV: 36.64 V, $I_{D(MAX)}$: 1.7992 A.

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10.3.4.4 10% Load – 5 V Output Diode (D4)

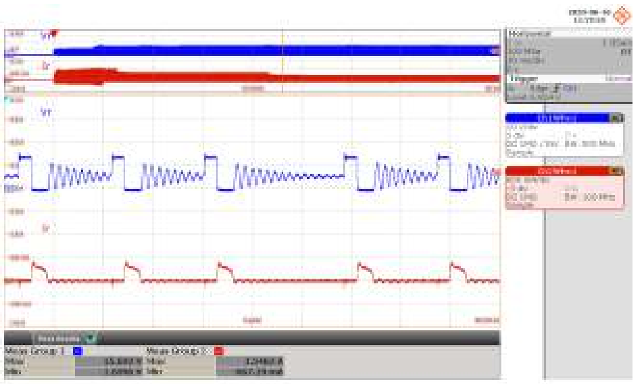

Figure 75 – 85 VAC / 60 Hz 10% Load.
CH 1: V_{R_D4}, 10 V / div., 10 ms. / div.
CH 4: I_{D4}, 800 mA / div., 10 ms. / div.
Zoom: 8 µs / div.
PIV: 15.692 V, $I_{D(MAX)}$: 1.5462 A.

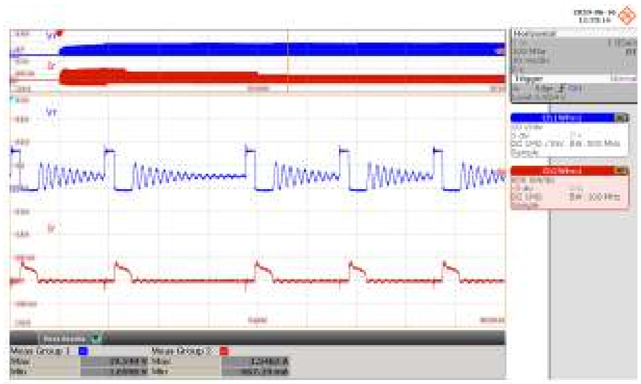

Figure 76 – 115 VAC / 60 Hz 10% Load.
CH 1: V_{R_D4}, 10 V / div., 10 ms. / div.
CH 4: I_{D4}, 800 mA / div., 10 ms. / div.
Zoom: 8 µs / div.
PIV: 19.249 V, $I_{D(MAX)}$: 1.5462 A.

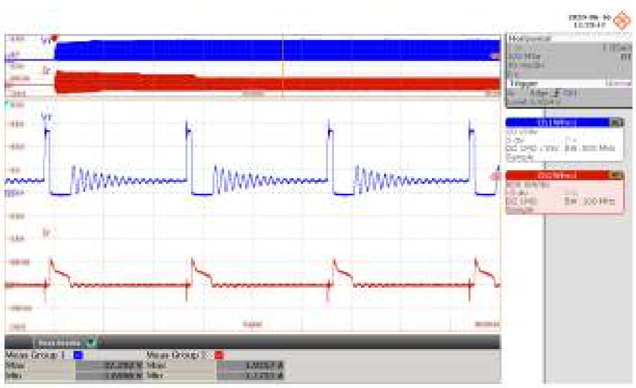

Figure 77 – 230 VAC / 50 Hz 10% Load.
CH 1: V_{R_D4}, 10 V / div., 10 ms. / div.
CH 4: I_{D4}, 800 mA / div., 10 ms. / div.
Zoom: 8 µs / div.
PIV: 32.292 V, $I_{D(MAX)}$: 1.9257 A.

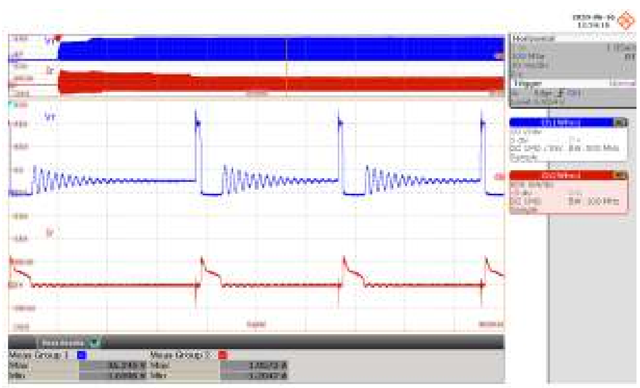

Figure 78 – 265 VAC / 50 Hz 10% Load.
CH 1: V_{R_D4}, 10 V / div., 10 ms. / div.
CH 4: I_{D4}, 800 mA / div., 10 ms. / div.
Zoom: 8 µs / div.
PIV: 36.245 V, $I_{D(MAX)}$: 1.9573 A.

10.4 ***Brown-In and Brown-Out***

10.4.1 12 V Output Response

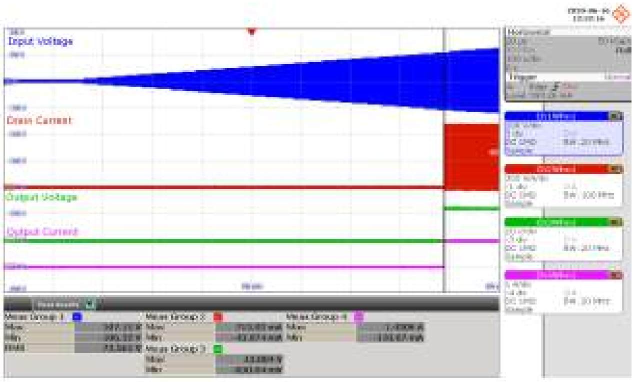

Figure 79 – Brown-In.
Channel 1: V_{IN}, 100 V / div., 100 s / div.
Channel 2: I_{DS}, 300 mA / div.
Channel 3: 12 V_{OUT}, 10 V / div.
Channel 4: 12 V I_{OUT}, 1 A / div.
V_{IN} = 73.561 VAC.

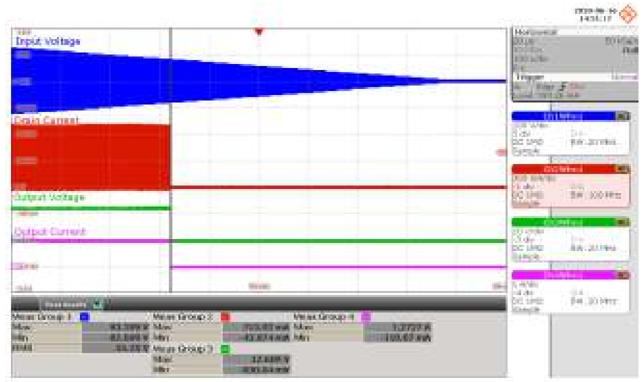

Figure 80 – Brown-Out.
Channel 1: V_{IN}, 100 V / div., 100 s / div.
Channel 2: I_{DS}, 300 mA / div.
Channel 3: 12 V_{OUT}, 10 V / div.
Channel 4: 12 V I_{OUT}, 1 A / div.
V_{IN} = 55.25 VAC.

10.4.2 5 V Output Response

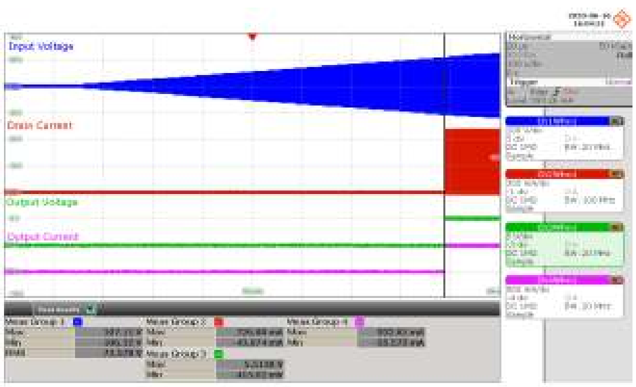

Figure 81 – Brown-In.
Channel 1: V_{IN}, 100 V / div., 100 s / div.
Channel 2: I_{DS}, 300 mA / div.
Channel 3: 5 V_{OUT}, 5 V / div.
Channel 4: 5 V I_{OUT}, 500 mA / div.
V_{IN} = 73.578 VAC.

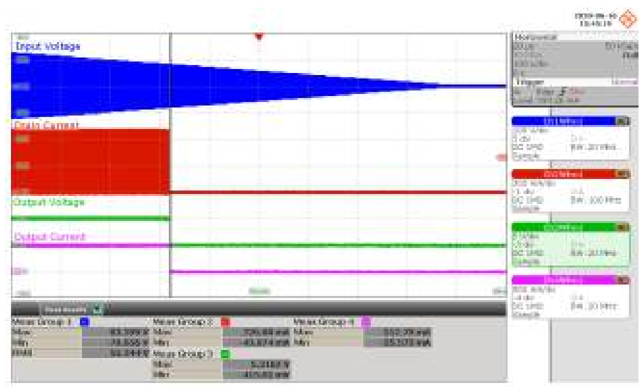

Figure 82 – Brown-Out.
Channel 1: V_{IN}, 100 V / div., 100 s / div.
Channel 2: I_{DS}, 300 mA / div.
Channel 3: 5 V_{OUT}, 5 V / div.
Channel 4: 5 V I_{OUT}, 500 mA / div.
V_{IN} = 55.244 VAC.

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10.5 ***Output Voltage Ripple***

10.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

Figure 83 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

Figure 84 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

10.5.2 Measurement Results

10.5.2.1 100% Load Condition – 12 V Output

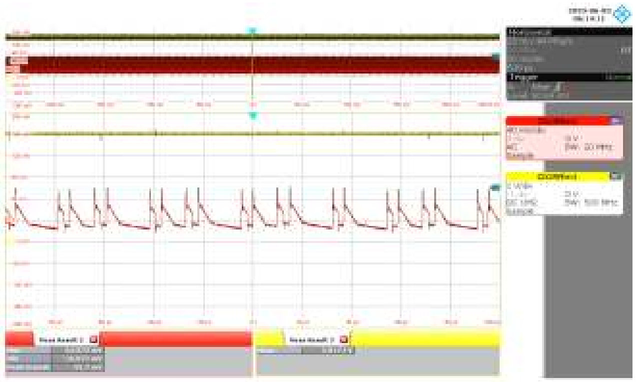

Figure 85 – 85 VAC / 60 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 1 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 91.7 mV.

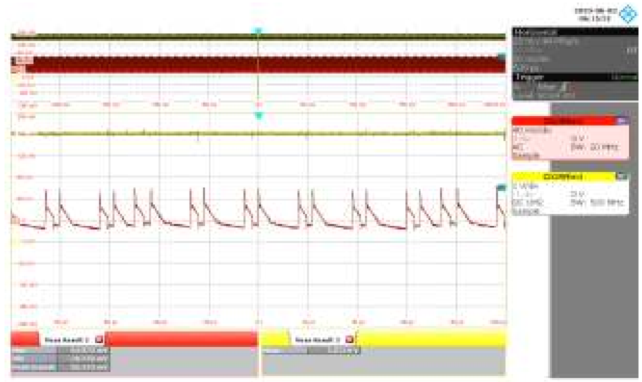

Figure 86 – 115 VAC / 60 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 1 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 85.375 mV.

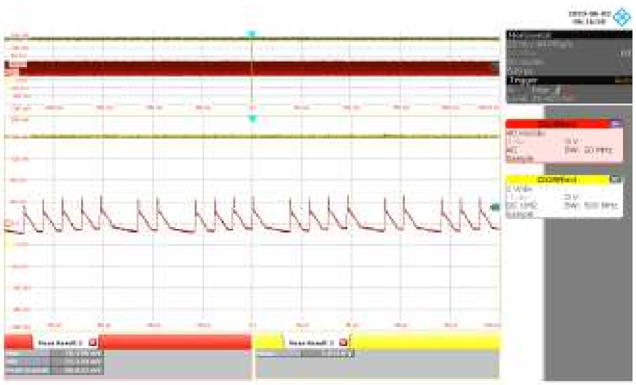

Figure 87 – 230 VAC / 50 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 1 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 80.632 mV.

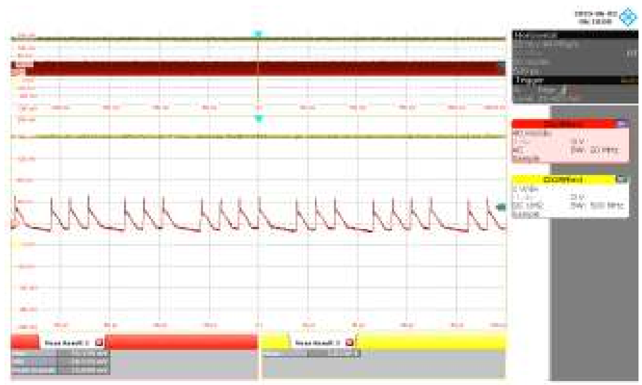

Figure 88 – 265 VAC / 50 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 1 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 75.889 mV.

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10.5.2.2 75% Load Condition – 12 V Output

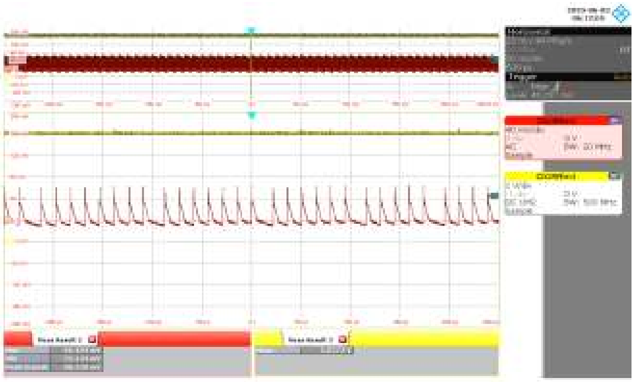

Figure 89 – 85 VAC / 60 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 1 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 88.538 mV.

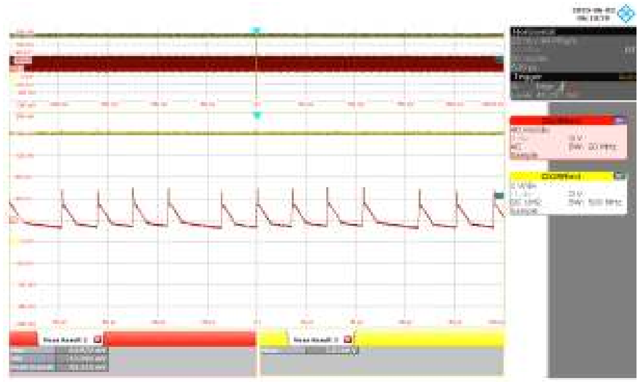

Figure 90 – 115 VAC / 60 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 1 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 82.213 mV.

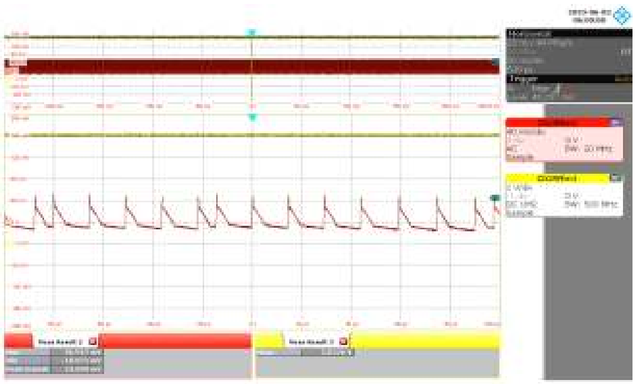

Figure 91 – 230 VAC / 50 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 1 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 75.889 mV.

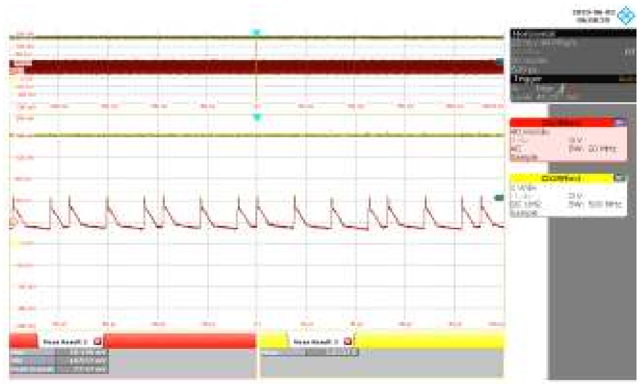

Figure 92 – 265 VAC / 50 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 1 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 77.47 mV.

10.5.2.3 50% Load Condition – 12 V Output

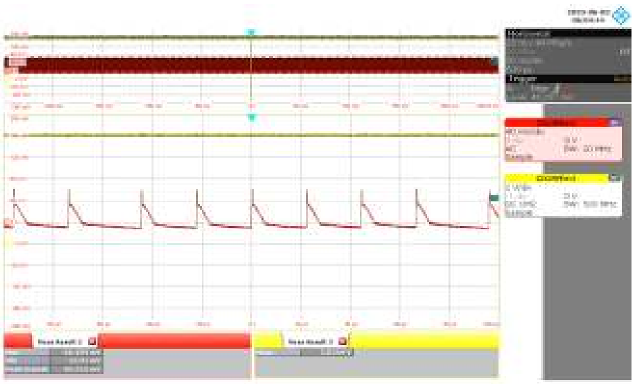

Figure 93 – 85 VAC / 60 Hz / 60 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 1 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 82.213 mV.

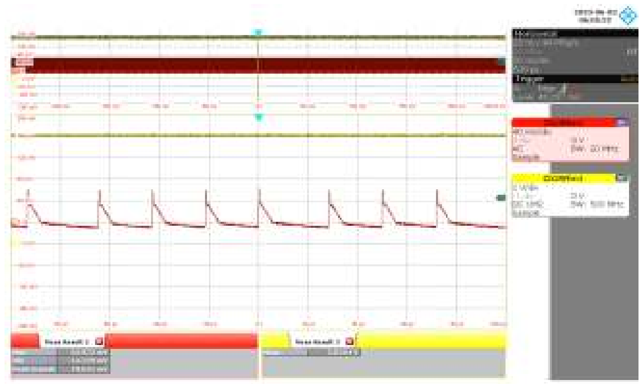

Figure 94 – 115 VAC / 60 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 1 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 79.051 mV.

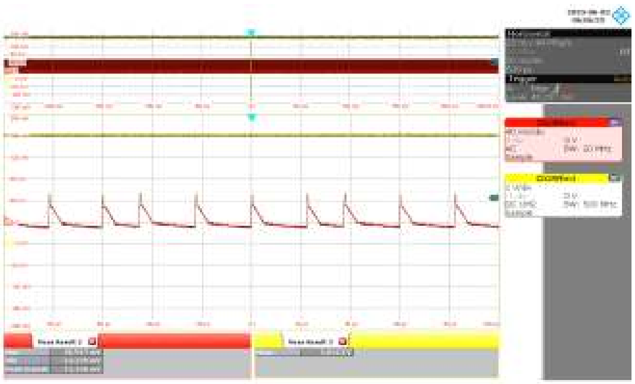

Figure 95 – 230 VAC / 50 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 1 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 71.146 mV.

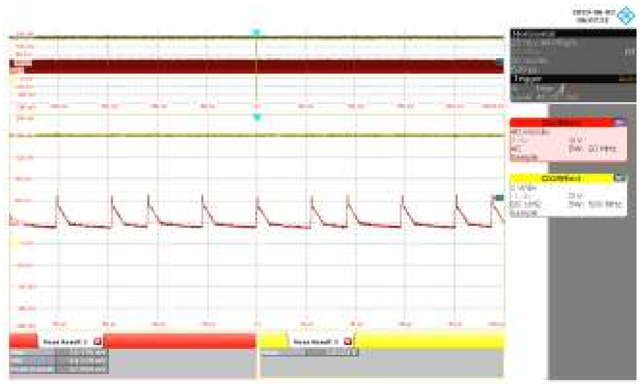

Figure 96 – 265 VAC / 50 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 1 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 67.984 mV.

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10.5.2.4 25% Load Condition – 12 V Output

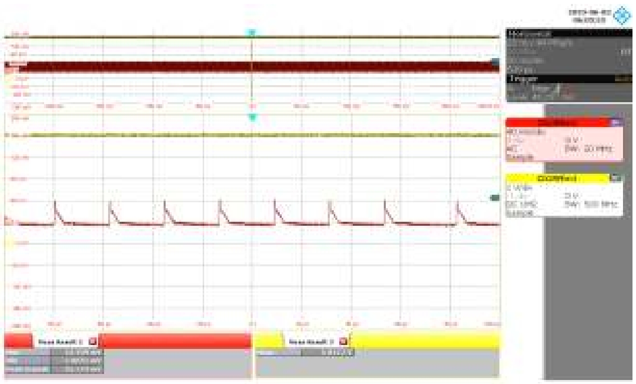

Figure 97 – 85 VAC / 60 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 1 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 52.174 mV.

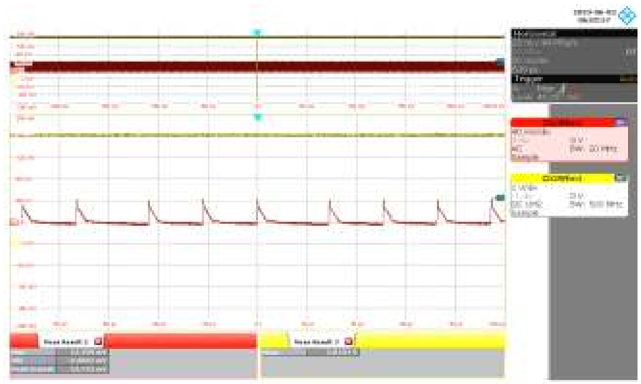

Figure 98 – 115 VAC / 60 Hz**.**
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 1 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 53.755 mV.

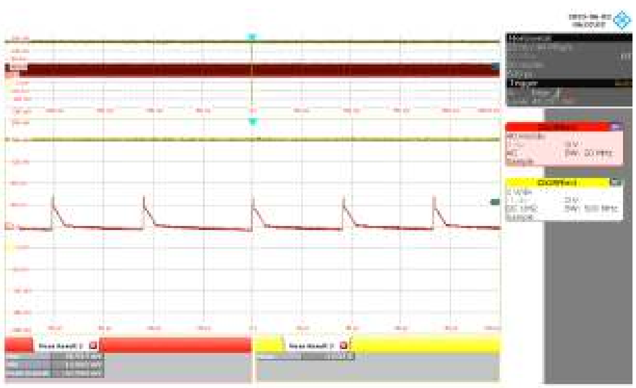

Figure 99 – 230 VAC / 50 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. /div.
CH 3: 5 V_{OUT}, 1 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 67.984 mV.

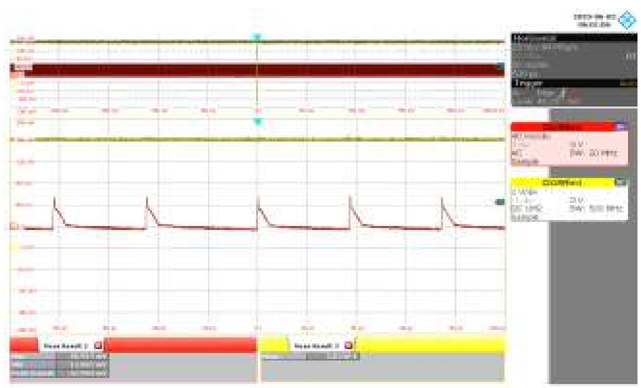

Figure 100 – 265 VAC / 50 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 1 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 67.984 mV.

10.5.2.5 10% Load Condition – 12 V Output

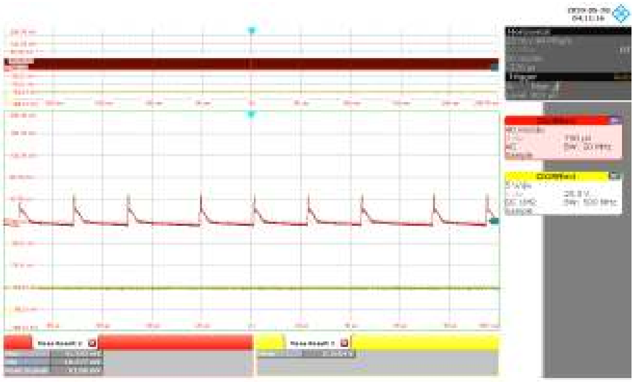

Figure 101 – 85 VAC / 60 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 5 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 61.66 mV.

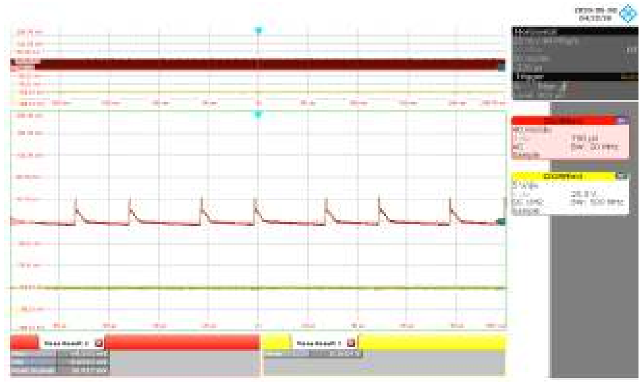

Figure 102 – 115 VAC / 60 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 5 V / div., 50 ms. / div.
Zoom: 20 µs / div.
12 V_{OUT} Output Ripple: 56.917 mV.

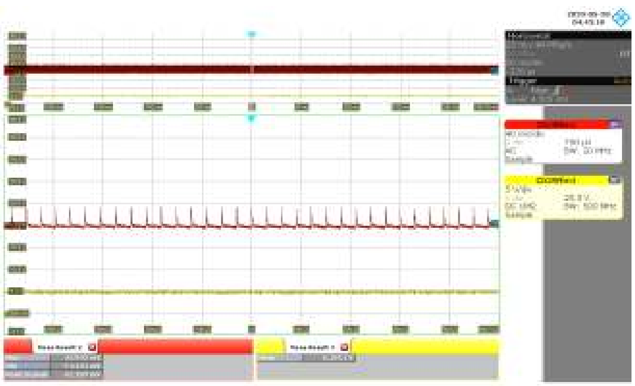

Figure 103 – 230 VAC / 50 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 5 V / div., 50 ms. / div.
Zoom: 100 µs / div.
12 V_{OUT} Output Ripple: 41.107 mV.

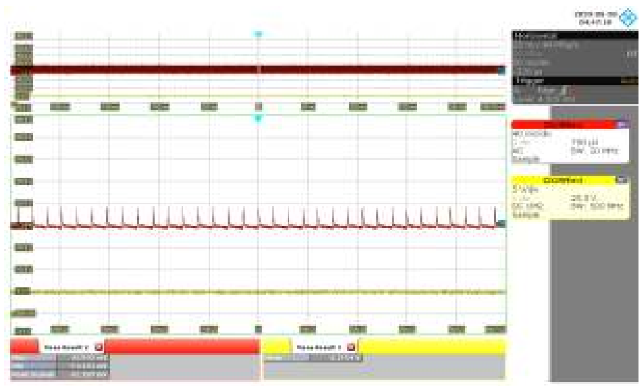

Figure 104 – 265 VAC / 50 Hz.
CH 2: 12 V_{OUT}, 40 mV / div., 50 ms. / div.
CH 3: 5 V_{OUT}, 5 V / div., 50 ms. / div.
Zoom: 100 µs / div.
12 V_{OUT} Output Ripple: 41.107 mV.

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10.5.2.6 100% Load Condition – 5 V Output

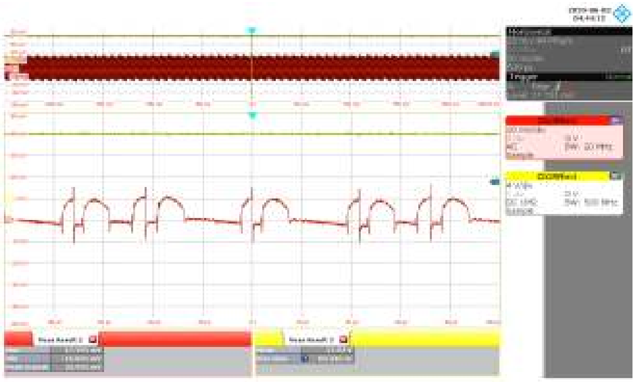

Figure 105 – 85 VAC / 60 Hz.
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 4 V / div., 50 ms. / div.
Zoom: 10 μs / div.
5 V_{OUT} Output Ripple: 33.992 mV.

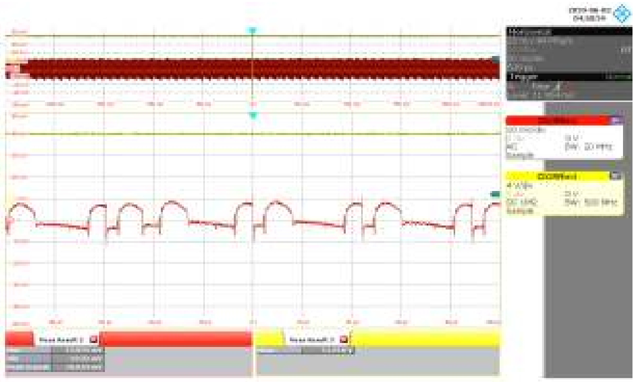

Figure 106 – 115 VAC / 60 Hz.
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 4 V / div., 50 ms. / div.
Zoom: 10 μs / div.
5 V_{OUT} Output Ripple: 28.854 mV.

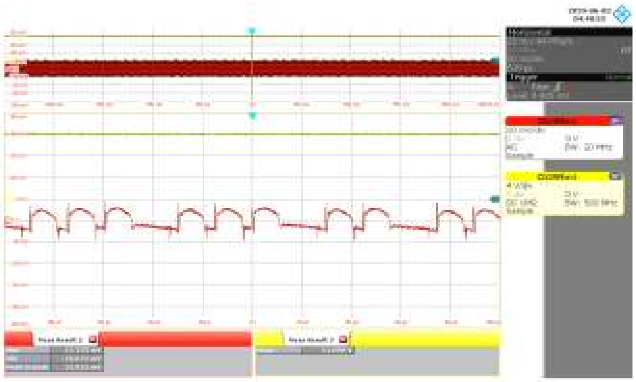

Figure 107 – 230 VAC / 50 Hz.
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 4 V / div., 50 ms. / div.
Zoom: 10 μs / div.
5 V_{OUT} Output Ripple: 22.925 mV.

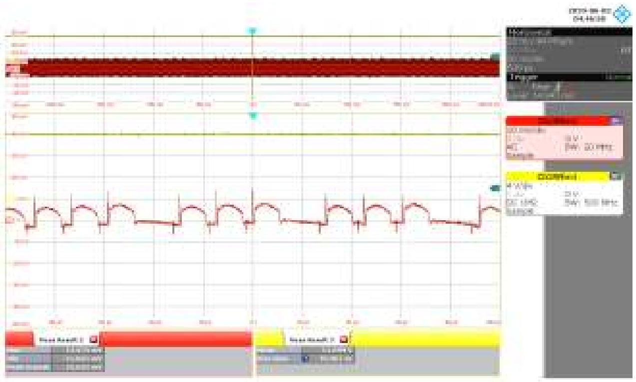

Figure 108 – 265 VAC / 50 Hz.
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 4 V / div., 50 ms. / div.
Zoom: 10 us / div.
5 V_{OUT} Output Ripple: 25.692 mV.

10.5.2.7 75% Load Condition – 5 V Output

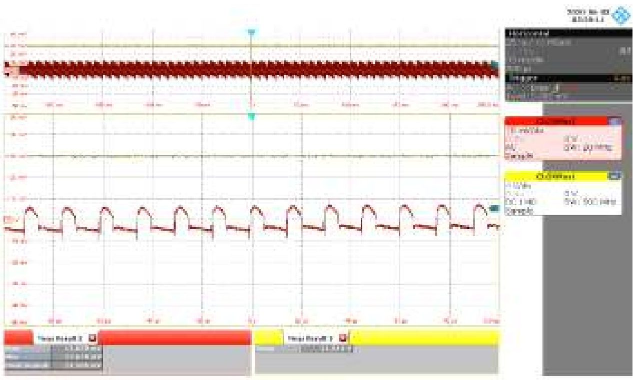

Figure 109 – 85 VAC / 60 Hz**.**
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 4 V / div., 50 ms. / div.
Zoom: 20 µs / div.
5 V_{OUT} Output Ripple: 24.506 mV.

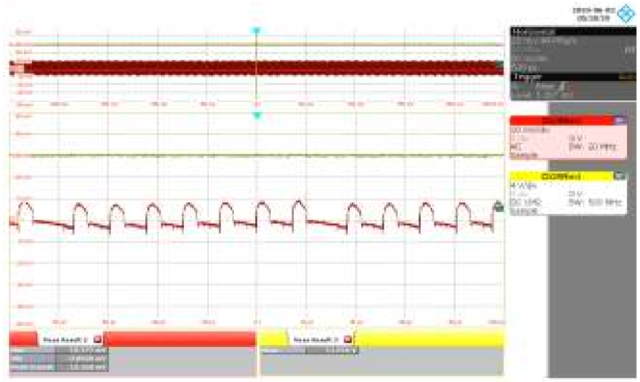

Figure 110 – 115 VAC / 60 Hz.
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 4 V / div., 50 ms. / div.
Zoom: 20 µs / div.
5 V_{OUT} Output Ripple: 19.368 mV.

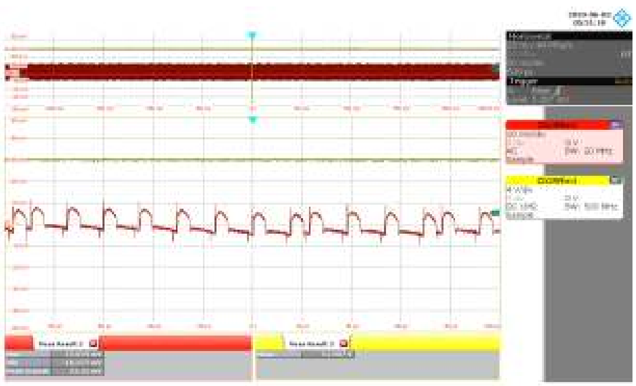

Figure 111 – 230 VAC / 50 Hz.
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 4 V / div., 50 ms. / div.
Zoom: 20 µs / div.
5 V_{OUT} Output Ripple: 23.32 mV.

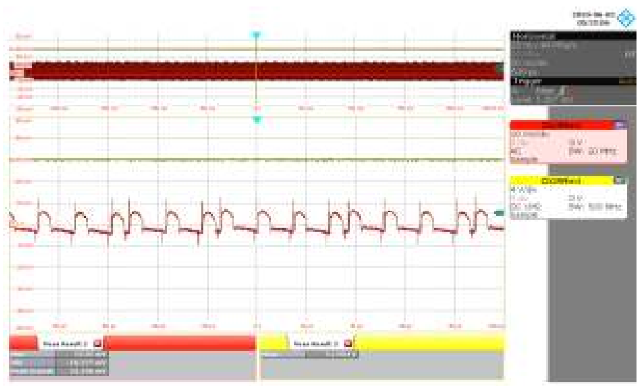

Figure 112 – 265 VAC / 50 Hz.
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 4 V / div., 50 ms. / div.
Zoom: 20 µs / div.
5 V_{OUT} Output Ripple: 25.296 mV.

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10.5.2.8 50% Load Condition – 5 V Output

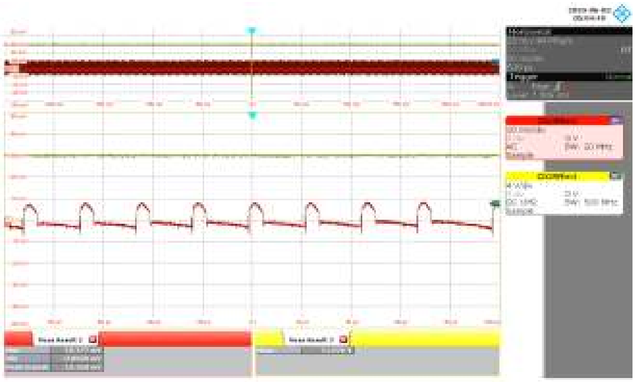

Figure 113 – 85 VAC / 60 Hz.
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 4 V / div., 50 ms. / div.
Zoom: 20 µs / div.
5 V_{OUT} Output Ripple: 19.368 mV.

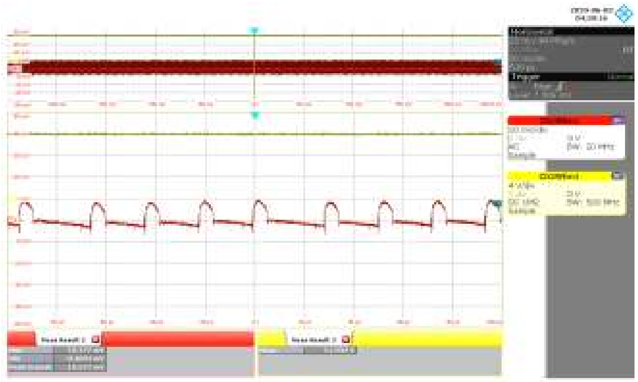

Figure 114 – 115 VAC / 60 Hz**.**
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 4 V / div., 50 ms. / div.
Zoom: 20 µs / div.
5 V_{OUT} Output Ripple: 18.577 mV.

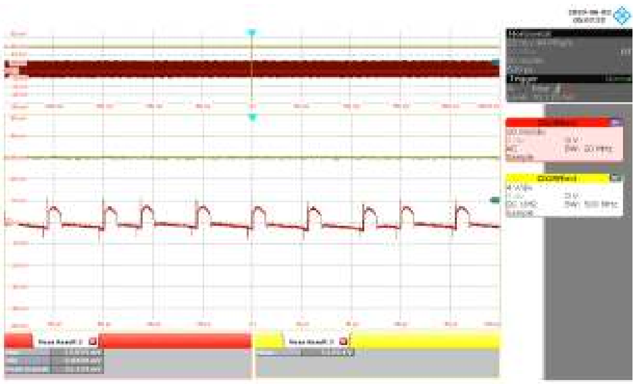

Figure 115 – 230 VAC / 50 Hz.
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 4 V / div., 50 ms. / div.
Zoom: 20 µs / div.
5 V_{OUT} Output Ripple: 22.134 mV.

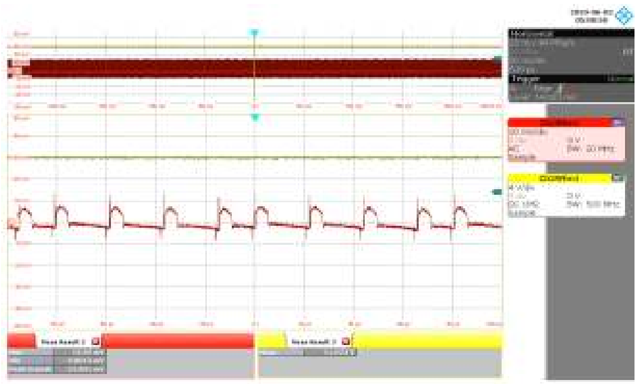

Figure 116 – 265 VAC / 50 Hz**.**
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 4 V / div., 50 ms. / div.
Zoom: 20 µs / div.
5 V_{OUT} Output Ripple: 24.901 mV.

10.5.2.9 25% Load Condition – 5 V Output

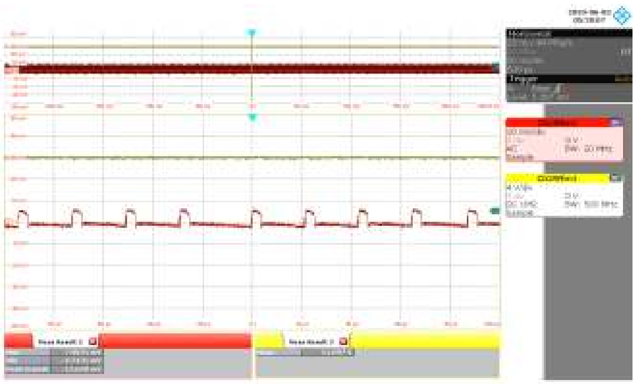

Figure 117 – 85 VAC / 60 Hz.
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 4 V / div., 50 ms. / div.
Zoom: 20 µs / div.
5 V_{OUT} Output Ripple: 12.648 mV.

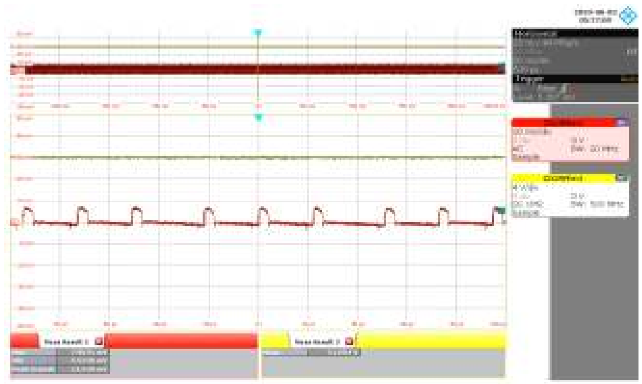

Figure 118 – 115 VAC / 60 Hz.
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 4 V / div., 50 ms. / div.
Zoom: 20 µs / div.
5 V_{OUT} Output Ripple: 13.439 mV.

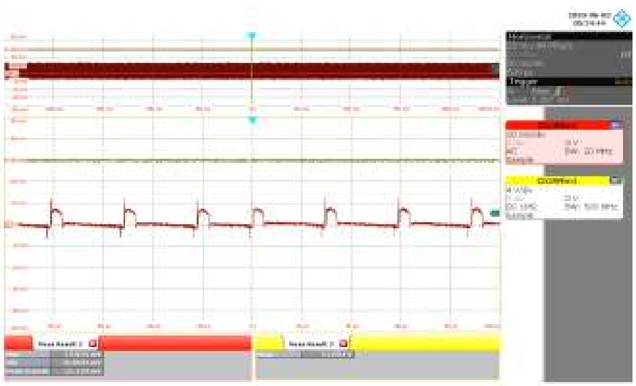

Figure 119 – 230 VAC / 50 Hz.
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 4 V / div., 50 ms. / div.
Zoom: 20 µs / div.
5 V_{OUT} Output Ripple: 22.134 mV.

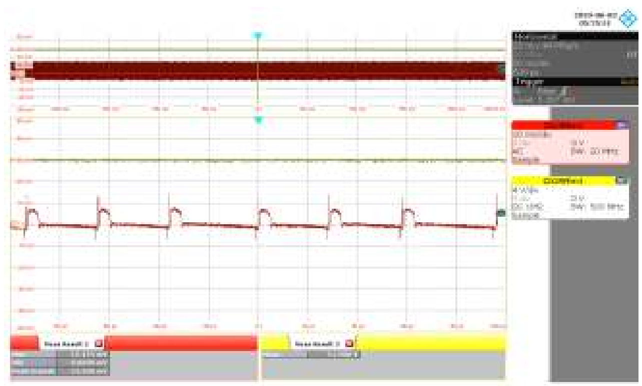

Figure 120 – 265 VAC / 50 Hz.
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 4 V / div., 50 ms. / div.
Zoom: 20 µs / div.
5 V_{OUT} Output Ripple: 24.506 mV.

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10.5.2.10 10% Load Condition – 5 V Output

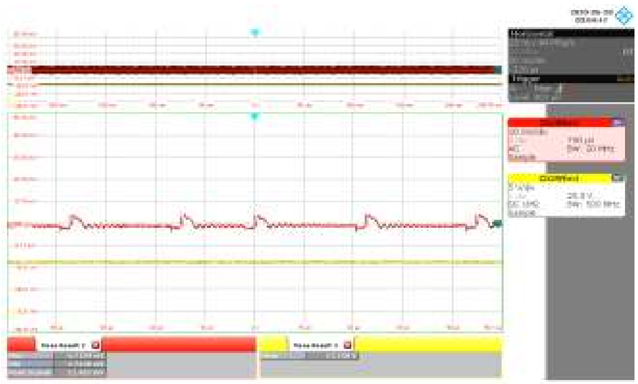

Figure 121 – 85 VAC / 60 Hz.
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 5 V / div., 50 ms. / div.
Zoom: 10 µs / div.
5 V_{OUT} Output Ripple: 11.462 mV.

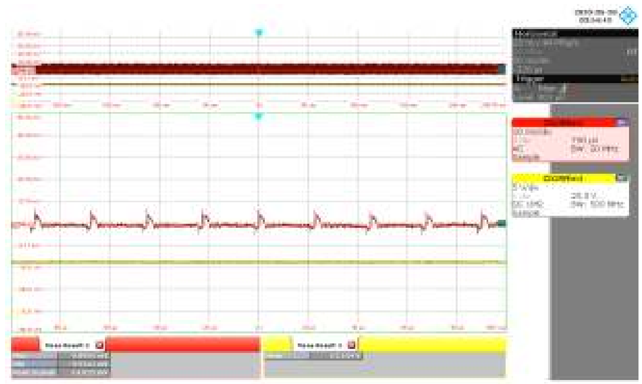

Figure 122 – 115 VAC / 60 Hz**.**
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 5 V / div., 50 ms. / div.
Zoom: 20 µs / div.
5 V_{OUT} Output Ripple: 14.625 mV.

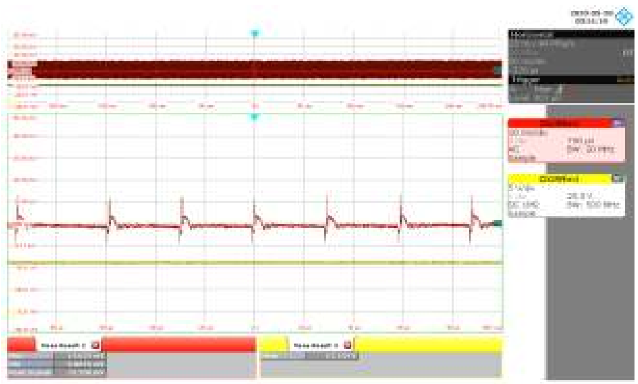

Figure 123 – 230 VAC / 50 Hz.
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 5 V / div., 50 ms. / div.
Zoom: 20 µs / div.
5 V_{OUT} Output Ripple: 24.506 mV.

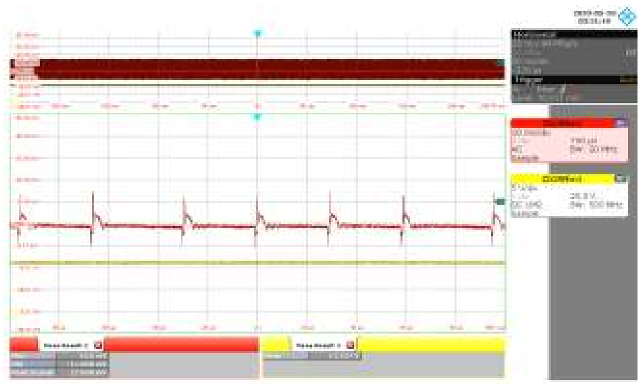

Figure 124 – 265 VAC / 50 Hz.
CH 2: 5 V_{OUT}, 10 mV / div., 50 ms. / div.
CH 3: 12 V_{OUT}, 5 V / div., 50 ms. / div.
Zoom: 20 µs / div.
5 V_{OUT} Output Ripple: 27.668 mV.

10.5.3 Output Ripple Voltage Graph from 0% - 100%

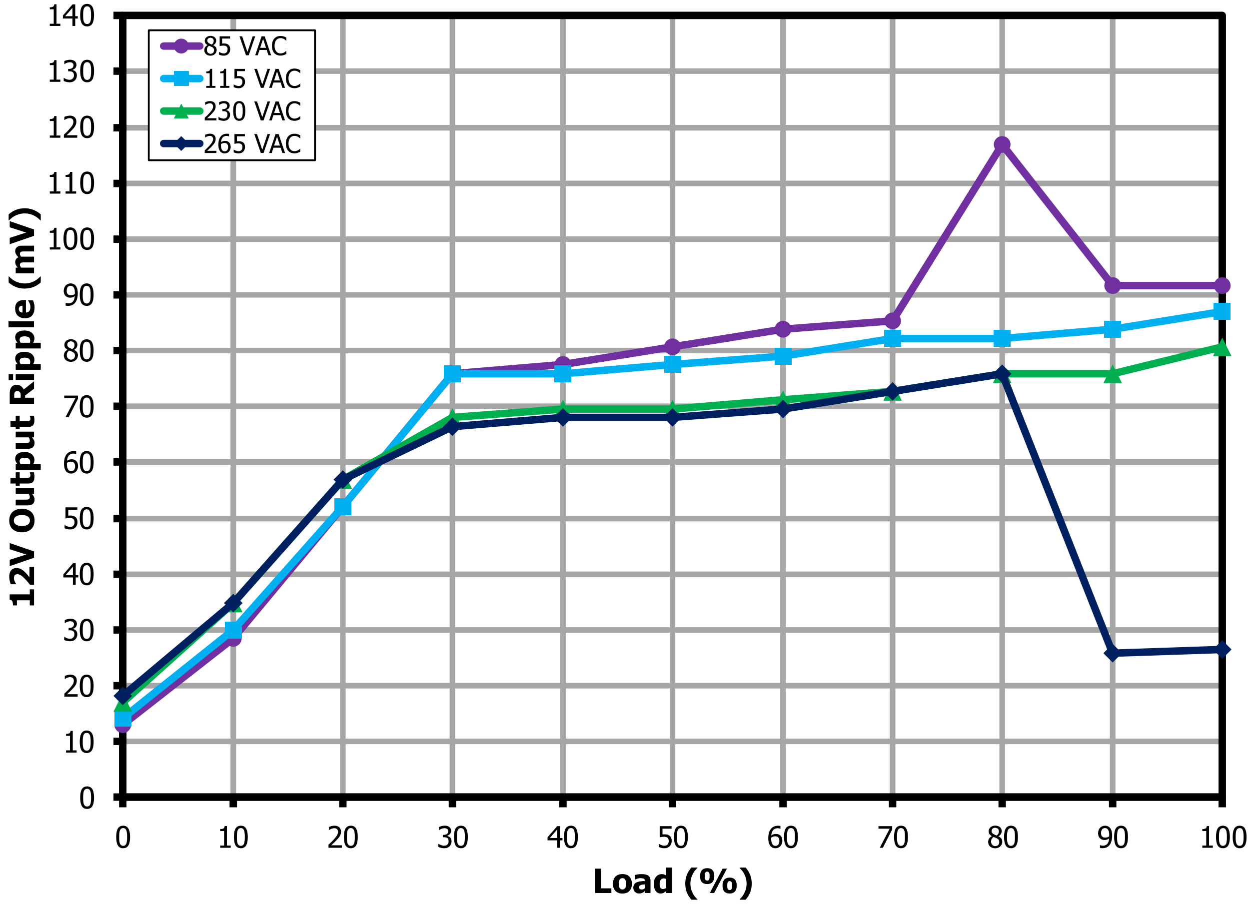

Figure 125 – 12 V Output Ripple Measured at the Board Output Terminals at Room Temperature.

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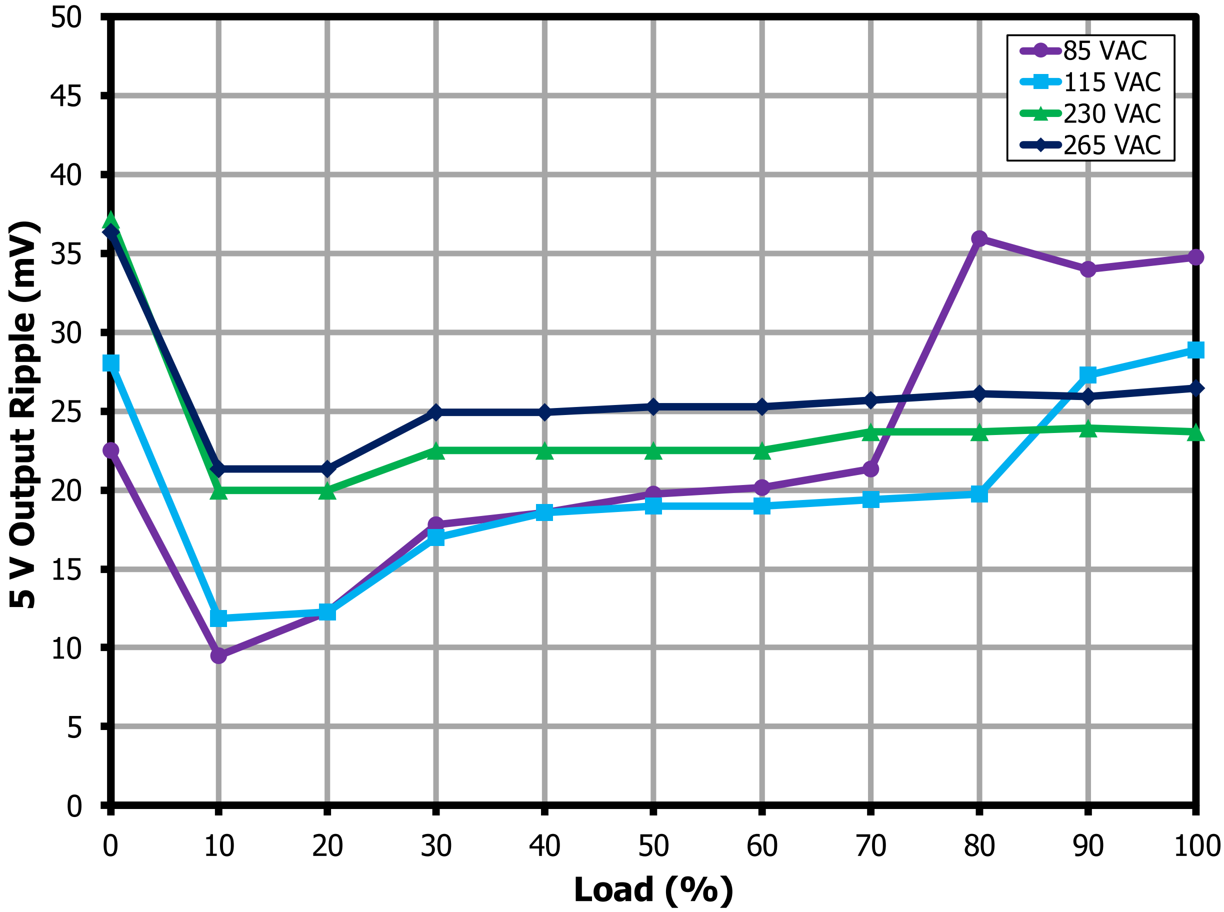

Figure 126 – 12 V Output Ripple Measured at the Board Output Terminals at Room Temperature.

11 Thermal Performance

11.1 *Test Set-Up*

Thermal evaluation was performed under two conditions: (1) room temperature with the circuit board enclosed inside an acrylic box and (2), 50 ºC ambient inside a thermal chamber. In both conditions, the circuit is soaked for two hours under full load conditions.

Note: In all thermal testing data, package D (SO-8C) was used instead of package P (DIP-8C).

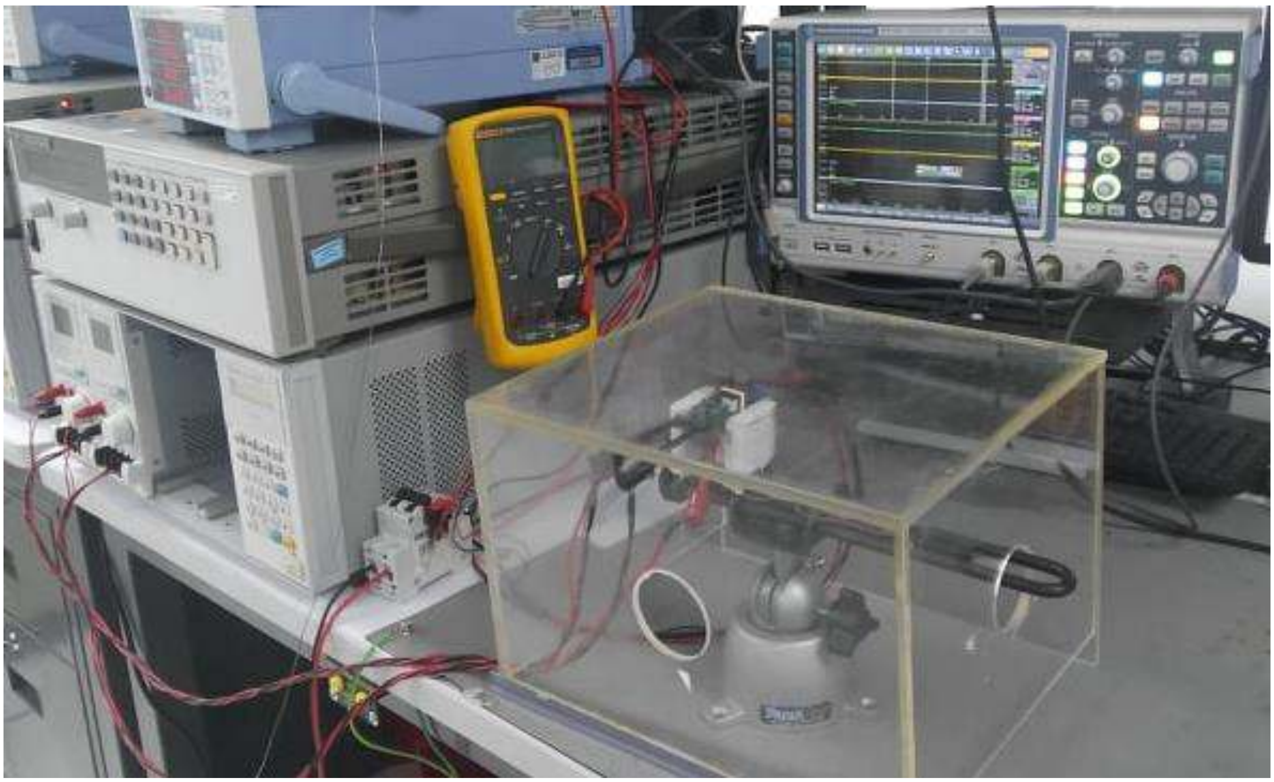

Figure 127 – Thermal Performance Set-up Using an Acrylic Box.

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Figure 128 – Thermal Performance Set-up Using Thermal Chamber.

11.2 *Thermal Performance at Room Temperature*

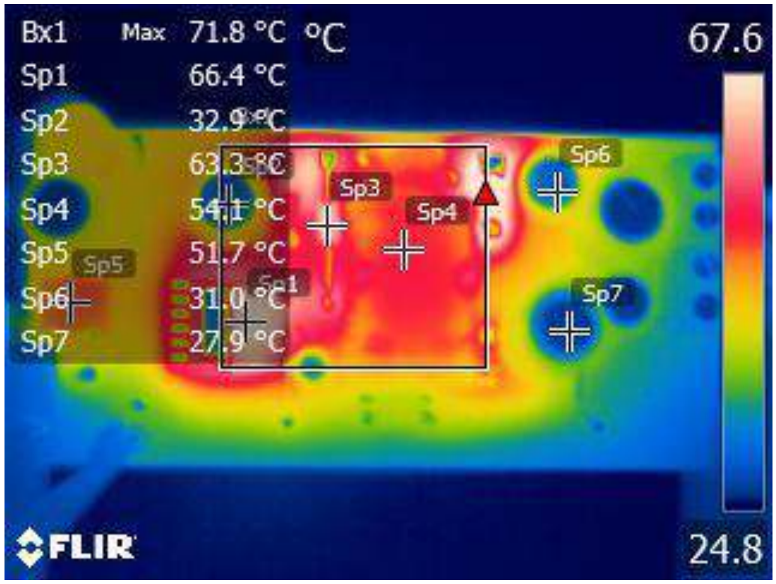

Figure 129 – Thermal Performance Top Side at 85 VAC, Full Load Using TNY289PG.

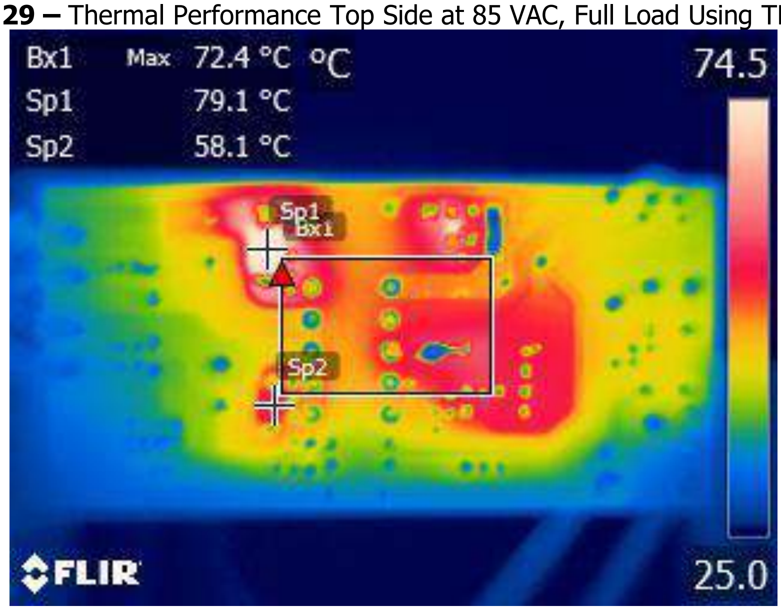

Figure 130 – Thermal Performance Bottom Side at 85 VAC, Full Load Using TNY289PG.

Component	Temperature (°C)
Bridge Rectifier (BR1)	51.7
Input Capacitor (C2)	32.9
Transformer (T1)	54.1
Primary Clamp Diode (D1)	63.3
TNY289 (U1)	66.4
12 V Output Capacitor (C13)	31.0
5 V Output Capacitor (C11)	27.9
Output Diode (D3)	79.1
Output Diode (D4)	58.1
Ambient	26.0

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11.2.1 265 VAC at Room Temperature

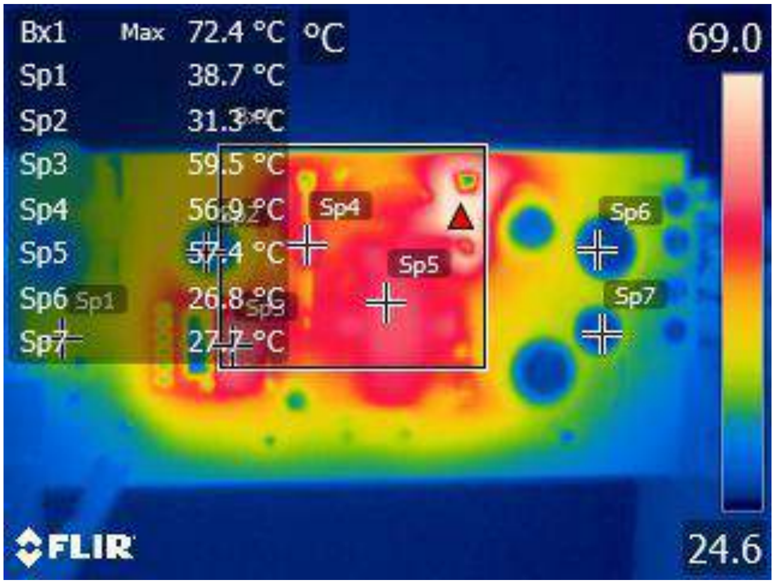

Figure 131 – Thermal Performance Top Side at 265 VAC, Full Load Using TNY289PG.

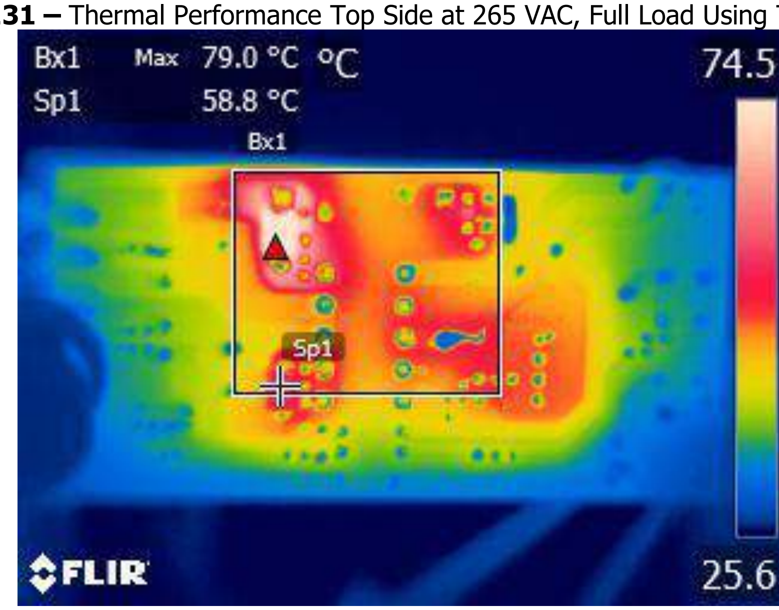

Figure 132 – Thermal Performance Bottom Side at 265 VAC, Full Load Using TNY289PG.

Component	Temperature (°C)
Bridge Rectifier (BR1)	38.7
Input Capacitor (C2)	31.3
Transformer (T1)	57.4
Primary Clamp Diode (D1)	56.9
TNY289 (U1)	59.5
12 V Output Capacitor (C13)	26.8
5 V Output Capacitor (C11)	27.7
Output Diode (D3)	79.0
Output Diode (D4)	58.8
Ambient	26.3

11.3 ***Thermal Performance at 50 °C***

11.3.1 85 VAC at 50 °C

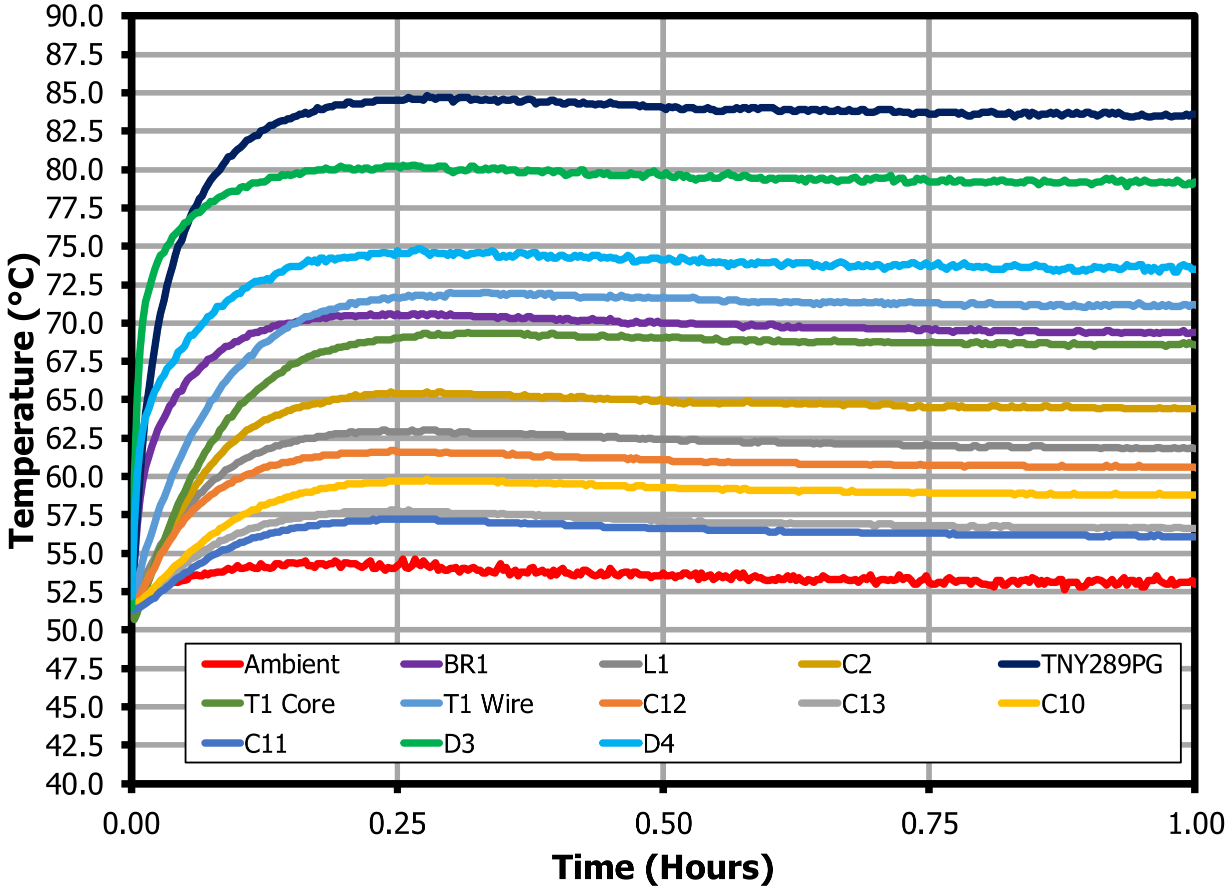

Figure 133 – Thermal Performance at 85 VAC, Full Load Using TNY289PG.

Component	Temperature (°C)
Bridge Rectifier (BR1)	69.2
Input Differential Mode Choke (L1)	61.7
Input Capacitor (C2)	64.3
Transformer (T1)	71.0
TNY289 (U1)	83.4
12 V Output Capacitor (C13)	60.5
5 V Output Capacitor (C11)	58.7
Output Diode (D3)	78.9
Output Diode (D4)	73.2
Ambient	52.7

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11.3.2 265 VAC at 50 °C

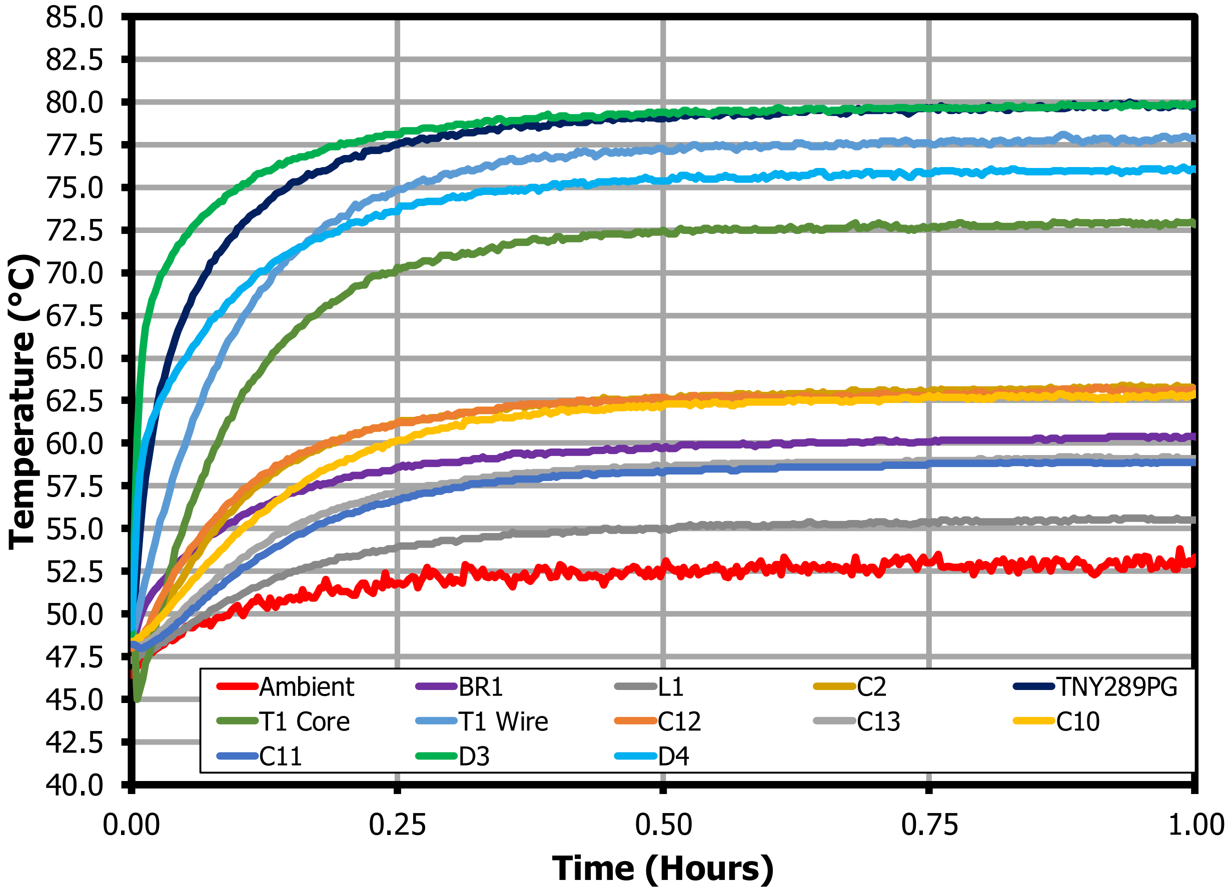

Figure 134 – Thermal Performance at 265 VAC, Full Load Using TNY289PG.

Component	Temperature (°C)
Bridge Rectifier (BR1)	60.3
Input Differential Mode Choke (L1)	55.5
Input Capacitor (C2)	63.3
Transformer (T1)	77.8
TNY289 (U1)	79.7
12 V Output Capacitor (C13)	63.1
5 V Output Capacitor (C11)	62.7
Output Diode (D3)	79.9
Output Diode (D4)	76.0
Ambient	52.6

11.4 *Over Temperature Protection*

11.4.1 OTP at 85 VAC

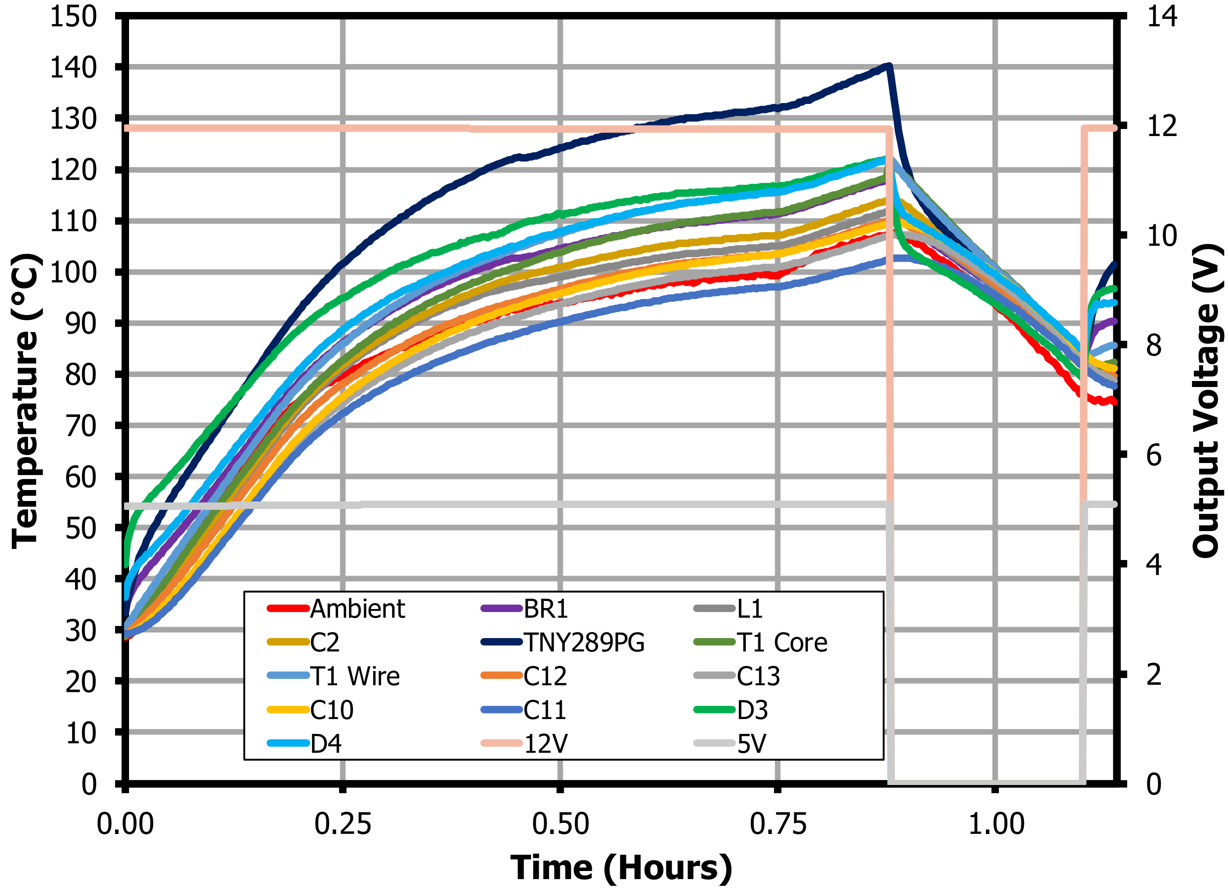

Figure 135 – Over Temperature Protection at 85 VAC Using TNY289PG.

Component	At OTP Trigger Temperature (°C)	At Recovery Temperature (°C)	Hysteresis
Ambient	107.5	75.4	32.1
Bridge Rectifier (BR1)	117.1	85	32.1
Input Capacitor (C2)	114.1	81.6	32.5
TNY289 (U1)	138	86.8	51.2
Transformer Core (T1)	121.2	81.3	39.9
Transformer Wire (T1)	121.9	83.4	38.5
Output Capacitor (C12)	110.2	80.6	29.6
Output Capacitor (C10)	109.6	83.5	26.1
Output Diode (D3)	118.1	88.3	29.8
Output Diode (D4)	119.2	89.5	29.7

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11.4.2 OTP at 265 VAC

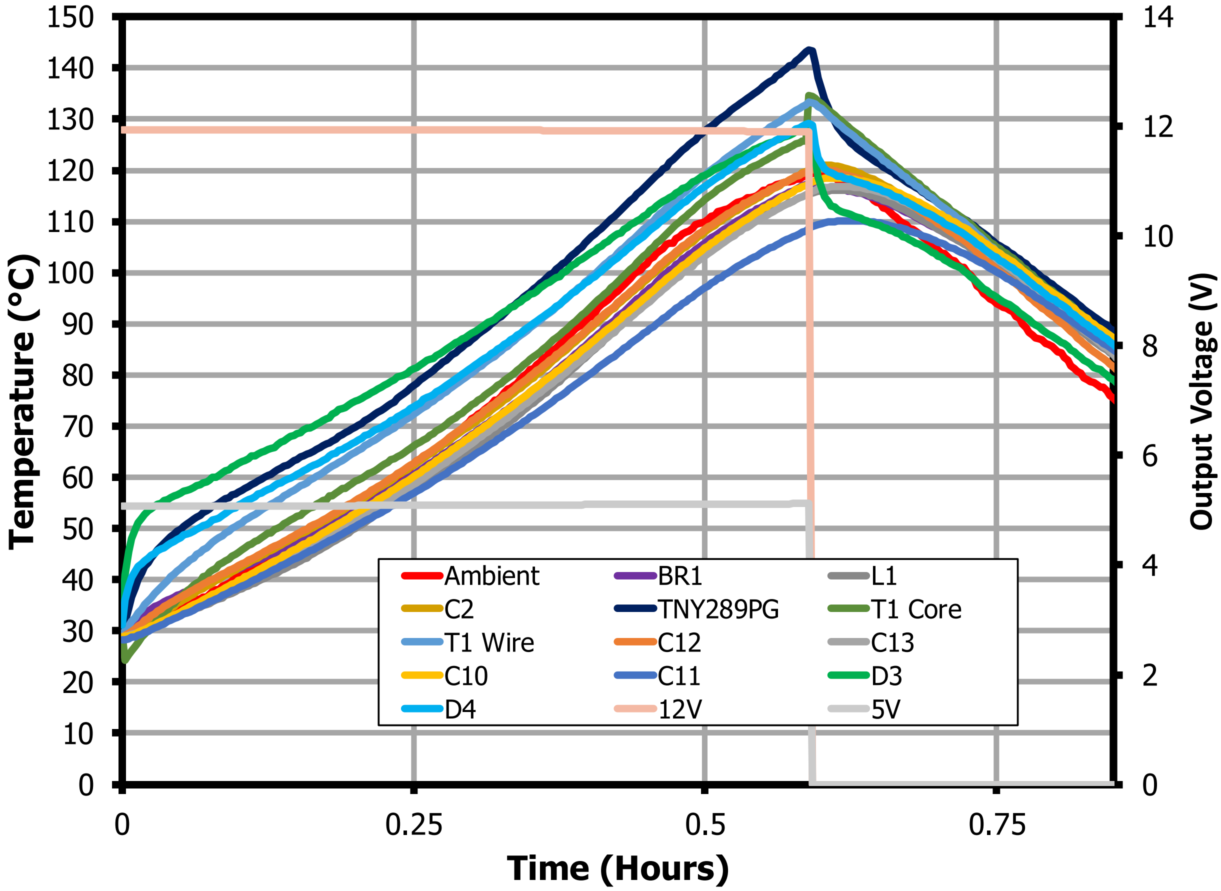

Figure 136 – Over Temperature Protection at 265 VAC Using TNY289PG.

Component	At OTP Trigger Temperature (°C)	At Recovery Temperature (°C)	Hysteresis
Ambient	119.2	69.7	49.5
Bridge Rectifier (BR1)	117.5	79.8	37.7
Input Capacitor (C2)	120.1	80.1	40
TNY289 (U1)	143.6	84.3	59.3
Transformer Core (T1)	134.6	74.9	59.7
Transformer Wire (T1)	133.3	79.9	53.4
Output Capacitor (C12)	119.9	75.3	44.6
Output Capacitor (C10)	117.4	81.1	36.3
Output Diode (D3)	128.2	80.7	47.5
Output Diode (D4)	129.2	84.5	44.7

12 Conducted EMI

Conducted emissions tests were performed at 115 VAC and 230 VAC at full load (12 V / 1 A, 5 V / 500 mA). Measurements were taken with a floating DC output load resistor. A DC output cable was included.

12.1 *Test Set-up Equipment*

12.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power Hi-tester.
4. Chroma measurement test fixture.
5. Input voltage set at 115 VAC and 230 VAC.

12.2 *Test Set-up*

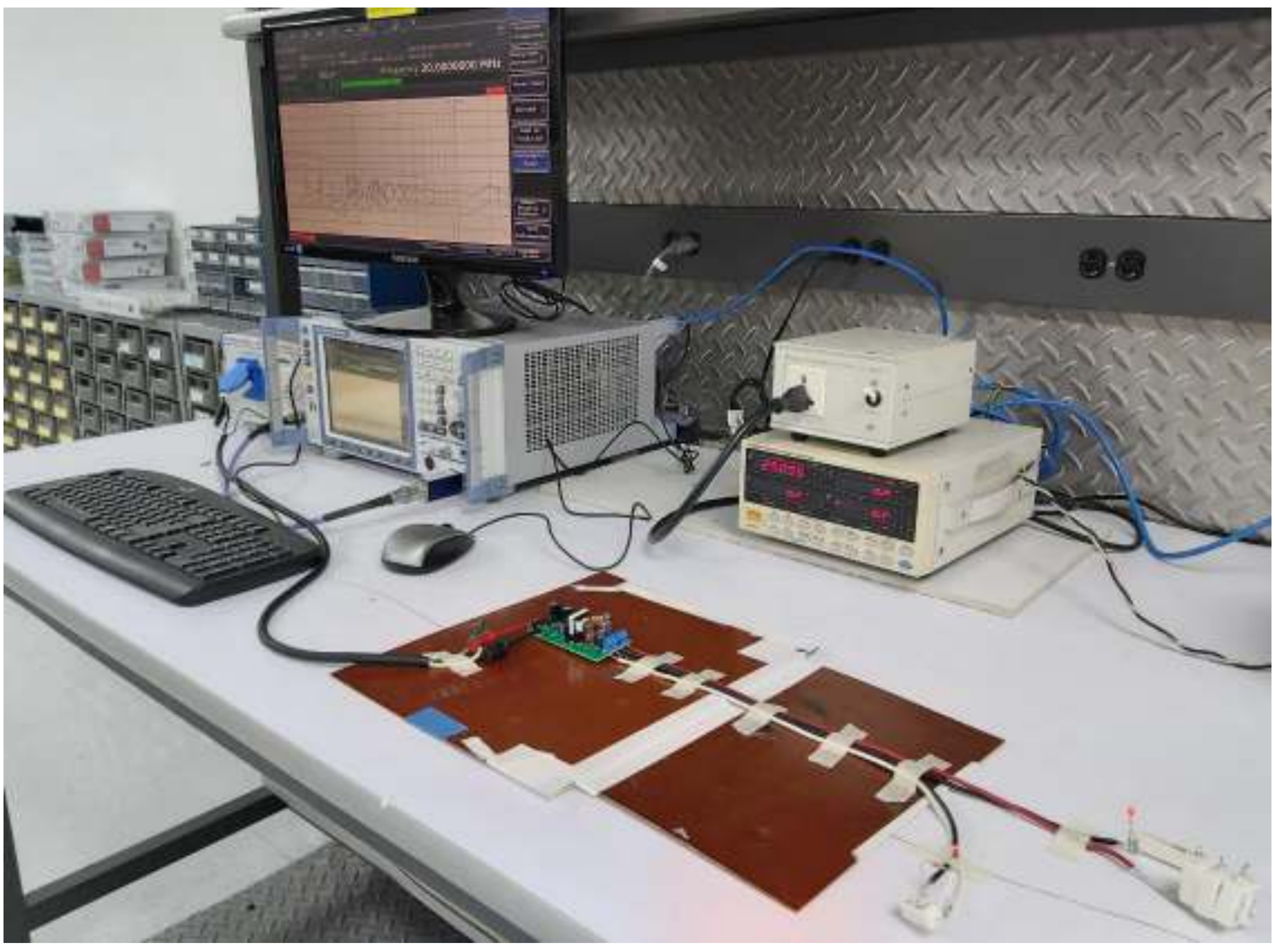

Figure 137 – EMI Test Set-up.

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12.3 *Test Results*

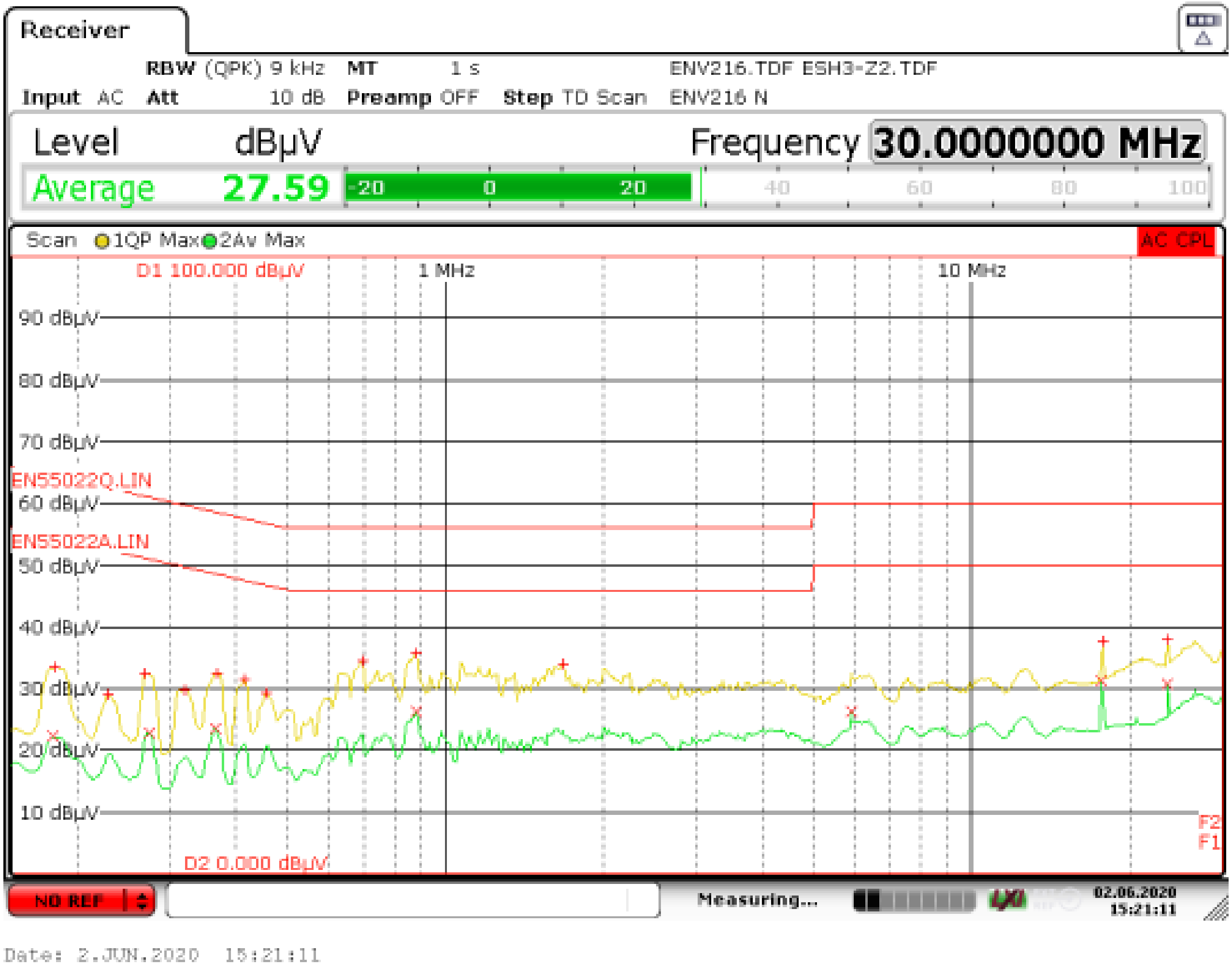
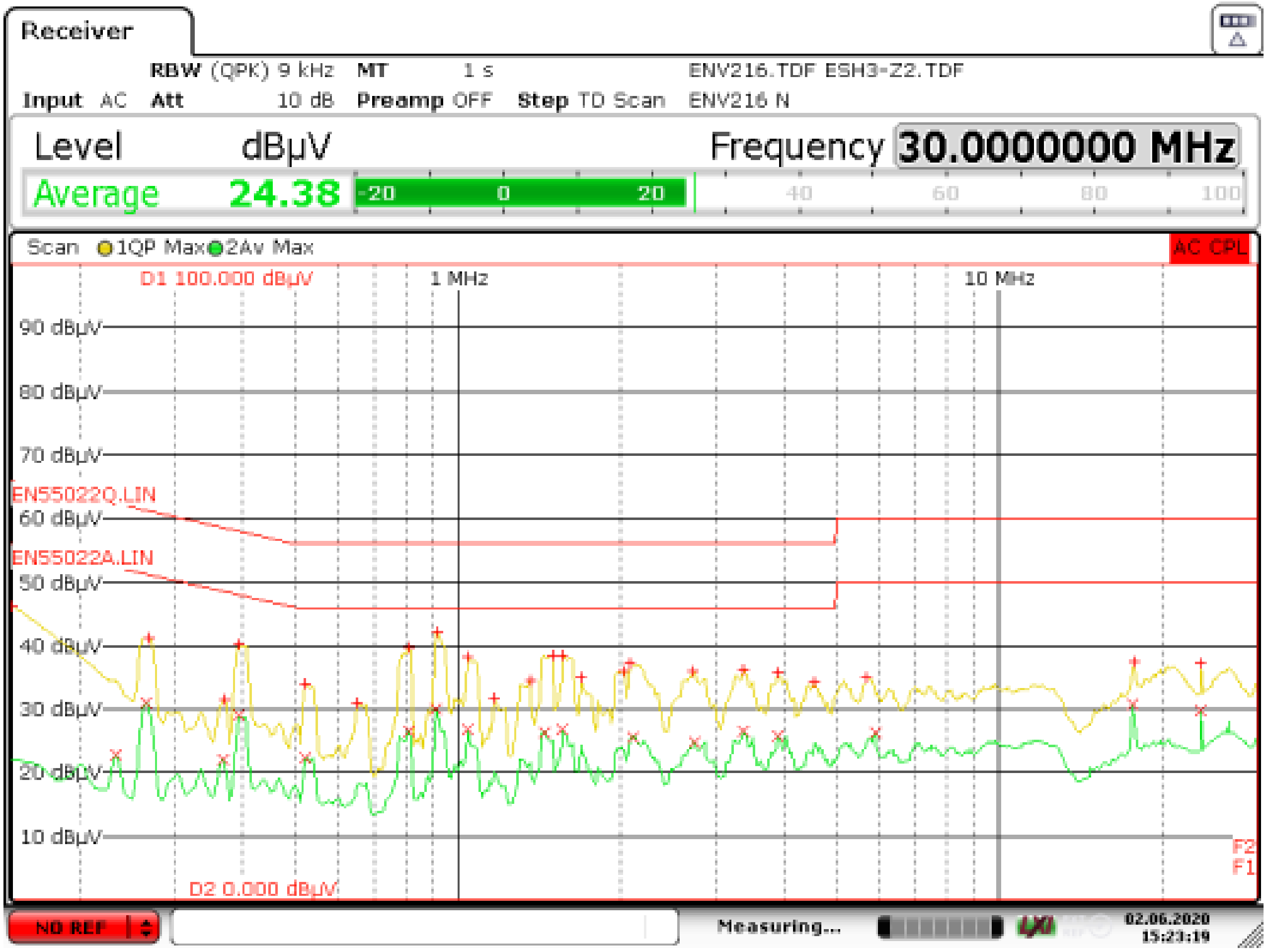


Figure 138 – 115 VAC 60 Hz, Line and Neutral.



Date: 2.JUN.2020 15:23:19

Figure 139 – 230 VAC 60 Hz, Line and Neutral.

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13 Line Surge

Differential and common mode input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

13.1 *Differential and Common Mode Surge*

DM Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+1000	230	L to N	0	Pass
-1000	230	L to N	0	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass
+1000	230	L to N	180	Pass
-1000	230	L to N	180	Pass
+1000	230	L to N	270	Pass
-1000	230	L to N	270	Pass

CM Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2000	230	L, N to PE	0	Pass
-2000	230	L, N to PE	0	Pass
+2000	230	L, N to PE	90	Pass
-2000	230	L, N to PE	90	Pass
+2000	230	L, N to PE	180	Pass
-2000	230	L, N to PE	180	Pass
+2000	230	L, N to PE	270	Pass
-2000	230	L, N to PE	270	Pass

Note: In all PASS results, no damage and no auto-restart was observed.

13.2 *Ring Wave*

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+3000	230	L, N to PE	0	Pass
-3000	230	L, N to PE	0	Pass
+3000	230	L, N to PE	90	Pass
-3000	230	L, N to PE	90	Pass
+3000	230	L, N to PE	180	Pass
-3000	230	L, N to PE	180	Pass
+3000	230	L, N to PE	270	Pass
-3000	230	L, N to PE	270	Pass

Note: In all PASS results, no damage and no auto-restart was observed.

13.3 *Electrical Fast Transient (EFT)*

Surge Level (V)	Injection Phase (°)	Frequency	T-Burst	T-Rep	Test Duration	Injection Location	Result (PASS,FAIL,AR)
+4000	0	2.5 kHz	30 ms	300 ms	120 s	L to N	Pass
-4000	0	2.5 kHz	30 ms	300 ms	120 s	L to N	Pass
+4000	0	5 kHz	15 ms	300 ms	120 s	L to N	Pass
-4000	0	5 kHz	15 ms	300 ms	120 s	L to N	Pass
+4000	0	100 kHz	750 μs	300 ms	120 s	L to N	Pass
-4000	0	100 kHz	750 μs	300 ms	120 s	L to N	Pass
+4000	90	2.5 kHz	30 ms	300 ms	120 s	L to N	Pass
-4000	90	2.5 kHz	30 ms	300 ms	120 s	L to N	Pass
+4000	90	5 kHz	15 ms	300 ms	120 s	L to N	Pass
-4000	90	5 kHz	15 ms	300 ms	120 s	L to N	Pass
+4000	90	100 kHz	750 μs	300 ms	120 s	L to N	Pass
-4000	90	100 kHz	750 μs	300 ms	120 s	L to N	Pass
+4000	270	2.5 kHz	30 ms	300 ms	120 s	L to N	Pass
-4000	270	2.5 kHz	30 ms	300 ms	120 s	L to N	Pass
+4000	270	5 kHz	15 ms	300 ms	120 s	L to N	Pass
-4000	270	5 kHz	15 ms	300 ms	120 s	L to N	Pass
+4000	270	100 kHz	750 μs	300 ms	120 s	L to N	Pass
-4000	270	100 kHz	750 μs	300 ms	120 s	L to N	Pass

Note: In all PASS results, no damage and no auto-restart was observed.

14 ESD

Passed ±8 kV contact discharge

Contact Voltage (kV)	Applied to	Number of Strikes	Test Result
+8	+12 V terminal	10	Pass
	RTN terminal	10	Pass
-8	+12 V terminal	10	Pass
	RTN terminal	10	Pass

Note: In all PASS results, no damage and no auto-restart was observed.

Passed ±15 KV Air discharge.

Air Discharge Voltage (kV)	Applied to	Number of Strikes	Test Result
+15	+12 V terminal	10	Pass
	RTN terminal	10	Pass
-15	+12 V terminal	10	Pass
	RTN terminal	10	Pass

Note: In all PASS results, no damage and no auto-restart was observed.

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15 Revision History

Date	Author	Revision	Description and Changes	Reviewed
24-Aug-20	JLS	1.0	Initial Release.	Apps & Mktg

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