Design Example Report

Title	***4.75 W Dual Output Power Supply Using LinkSwitch-TN2 LNK3206D***
Specification	Input: 85 VAC – 265 VAC Output: 18.0 V-250 mA, 5.0 V-50 mA
Application	Embedded Power Supply
Author	Applications Engineering Department
Document Number	DER-508
Date	November 8, 2016
Revision	1.0

Summary and Features

- Highly integrated solution
- Output voltage regulation, <±5%
- Programmable current limit selection feature of LinkSwitch-TN2 enables optimal inductor selection
- Extremely fast transient response independent of load timing
- >75% Efficiency at full load condition
- < 200 mW no-load input power at 230 VAC
- No optocoupler or Zener diode required for regulation

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a dual output 18 V, 250 mA and 5 V, 50 mA adapter utilizing a device from the LinkSwitch-TN2 family of ICs. This design shows the high power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

Figure 1 – Populated Circuit Board Photograph, Top.

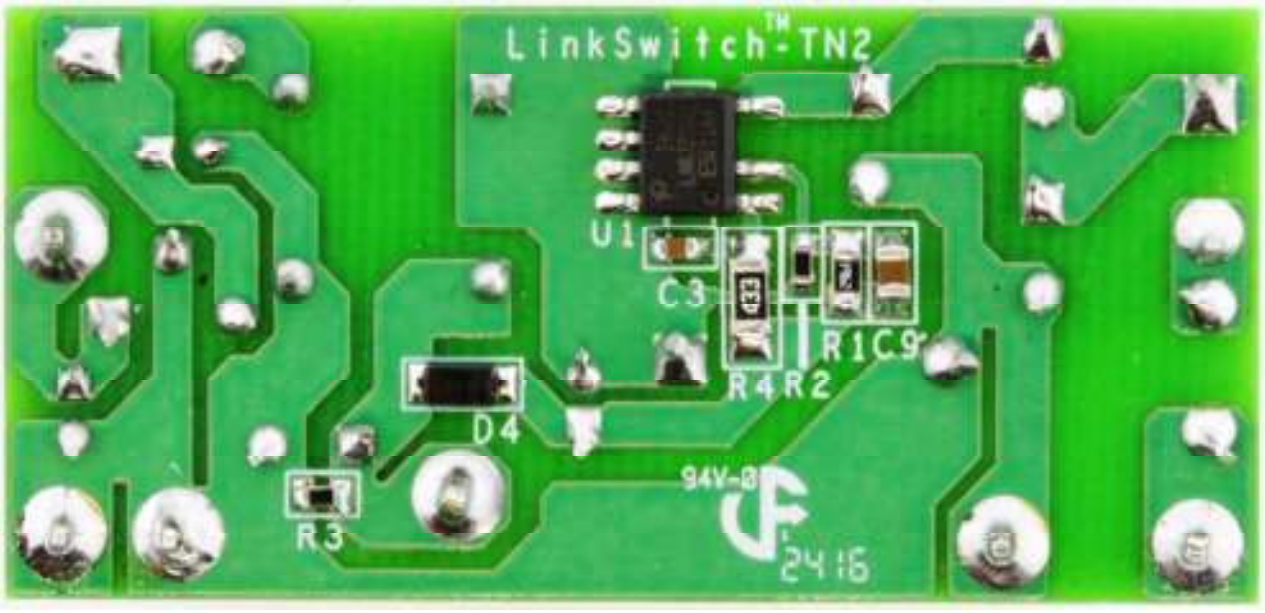

Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – No P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				200	mW	230 VAC.
Output						
Output Voltage 1	V_{OUT1}	17.1	18	18.9	V	±5%
Output Current 1	I_{OUT1}		250		mA	
Output Voltage Ripple 1	$V_{RIPPLE1}$			180	mV	20 MHz Bandwidth.
Output Voltage 2	V_{OUT2}	4.75	5	5.25	V	±5%
Output Current 2	I_{OUT2}		50		mA	
Output Voltage Ripple 2	$V_{RIPPLE2}$			50	mV	20 MHz Bandwidth.
Peak Power Output	P_{OUT_PEAK}	4.75			W	
Efficiency at 115 VAC / 230 VAC						
Full load	η	75			%	Measured at Output Terminal.
Environmental						
Conducted EMI			CISPR22B / EN55022B Floating			Resistive Load, 6 dB Margin.
Line Surge						
Differential Mode				1	kV	1.2 μs / 50 μs Surge Mode, 2 Ω.
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level in Sealed Enclosure.

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3 Schematic

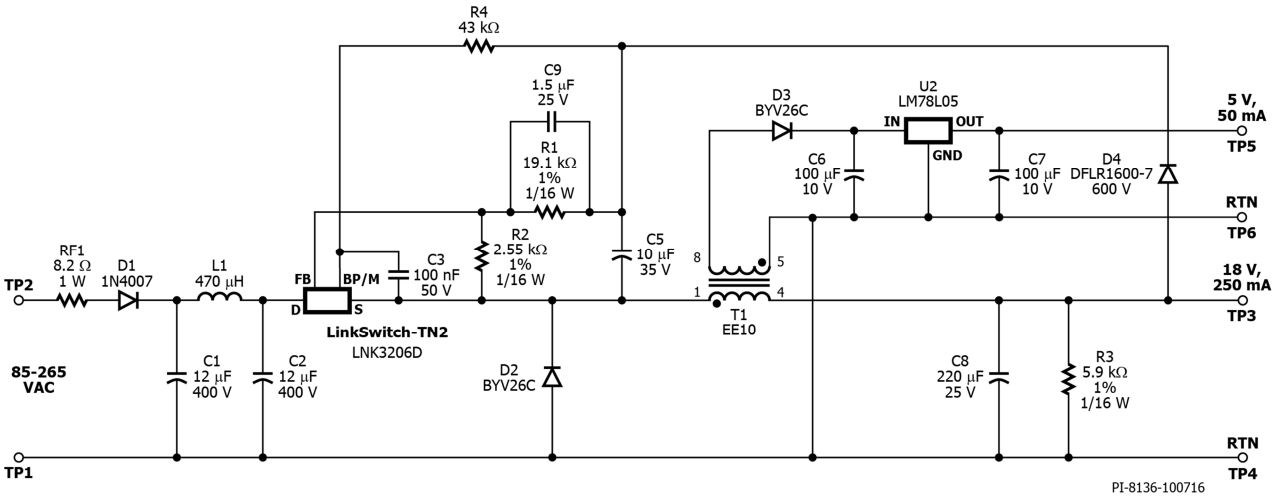

Figure 3 – Schematic.

4 Circuit Description

4.1 Input Rectifier and Filter

Input rectification is provided by diode D1. The rectified input is filtered by capacitors C1 and C2. The π (pi) filter comprising of inductor L1 and capacitors C1 and C2 provides filtering for differential mode EMI. EMI is further reduced by the integrated frequency jitter feature of the LinkSwitch-TN2 family of devices. Fusible resistor RF1 provides additional differential filtering and also protects by safely opening the circuit in case of catastrophic failure of any of the components in the circuit.

4.2 LinkSwitch-TN2 Primary Side and Main Output Circuit Operation

The LinkSwitch-TN2 device integrates a high-voltage power MOSFET, oscillator, ON/OFF controller, frequency jittering, startup and other protections on a single monolithic IC.

An internal current source from the DRAIN (D) pin of the LNK3206D IC U1, charges the capacitor C3 to provide control supply to the controller inside the IC. LinkSwitch-TN2 family of controllers work on the principle of ON-OFF control in which regulation is achieved by skipping cycles. During the power MOSFET off-time, capacitor C5 is charged to the output voltage via D4. This voltage is used to provide feedback to the IC via the resistor divider formed by resistors R1 and R2. The FEEDBACK (FB) pin is sampled by the controller inside U1 during each switching cycle. If current flowing into the FB pin is below 49 μA when the sampling occurs, controller switching is enabled for that particular switching cycle and the power MOSFET turns on. This will develop a linear ramp in current through inductor T1 and C8. Once the internal current limit is reached, the power MOSFET inside IC U1 is turned OFF and will remain OFF for the remaining portion of the switching cycle and the inductor current can freewheel via diode D2. The regulation of the main output is maintained by skipping cycles (ON/OFF control).

Diode D2 should be an ultrafast type diode with t_{RR} ≈ 25 ns. Although a slower diode may be used, this might cause higher reverse recovery current spikes at the turn ON of the power MOSFET inside U1 and reduce efficiency.

During full load operation, only a few switching cycles will be skipped (disabled), which results in a high effective switching frequency. As the load is reduced, more switching cycles are skipped which reduces the effective switching frequency. At no-load, most switching cycles are skipped and that makes the no-load power consumption of supplies designed using LinkSwitch-TN2 family low. Switching losses are the dominant loss mechanism at light loading and effective drop in switching frequency helps to improve light load efficiency. Additionally, since the amount of energy per switching cycle is fixed by I_{LIMIT}, the skipping of switching cycles gives the supply a nearly flat efficiency characteristic over the load range.

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LinkSwitch-TN2 family of devices do not require an external bias supply for operation and can be configured to be self-powered, however, providing the operating current for the device into the BYPASS (BP) pin externally, dramatically reduces no load input power. Resistor R4 connected from output sampling capacitor C5 to the BP pin provides the required supply current for the IC U1. To achieve lowest no-load power consumption, the current fed into the BP pin should be slightly higher than 120 μA. For the best full load efficiency and thermal performance, the current fed into the BP pin should be slightly higher than 290 μA however that will marginally increase the no load input power.

Capacitor C9 ensures stable operation.

4.3 Regulation of Additional Output

Additional auxiliary 5 V output is obtained using an additional winding on the inductor T1. This winding is rectified and filtered by diode D3 and capacitor C6. Diode D3 is a Schottky diode to reduce rectification loss.

Generally a 5 V or 3.3 V supply required for operating digital circuits in practical applications, requires regulation <5%. A low cost linear regulator IC U2 provides a regulated 5 V output. Capacitor C7 provides filtering for IC U2.

5 PCB Layout

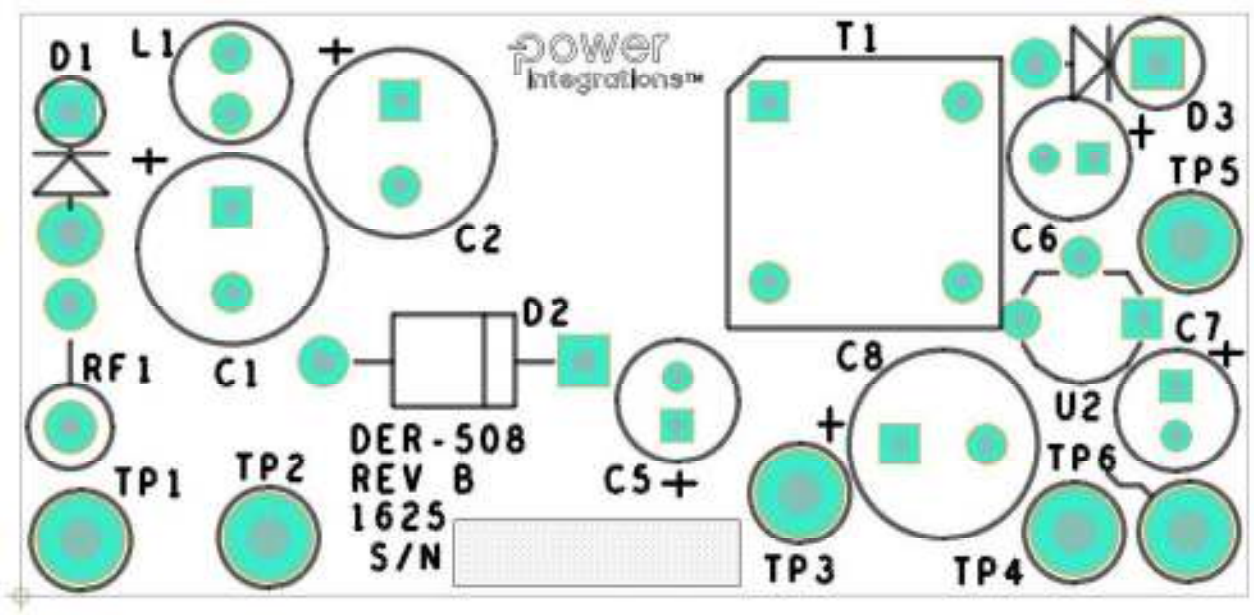

Figure 4 – Printed Circuit Layout, Top.

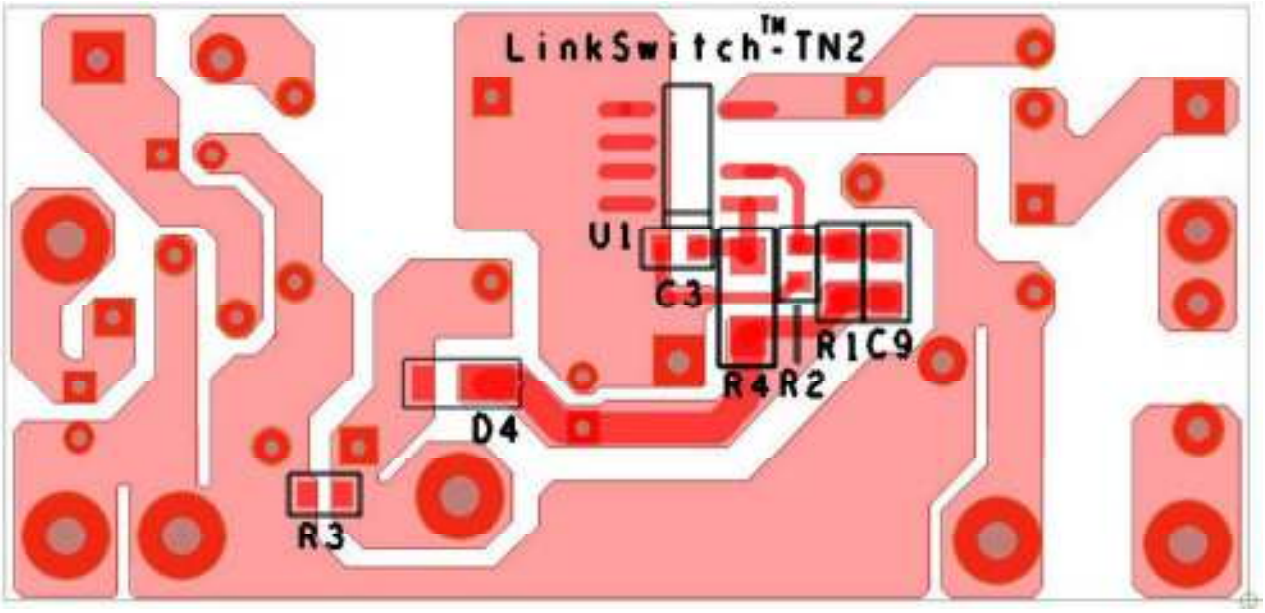

Figure 5 – Printed Circuit Layout, Bottom.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	C1 C2	12 µF, 400 V, Electrolytic, (8 x 16)	EKM126M2GF16RRS1P	Man-Yue Electronics
2	1	C3	100 nF 50 V, Ceramic, X7R, 0603	C1608X7R1H104K	TDK
3	1	C5	10 µF, 35 V, Electrolytic, Gen. Purpose, (5 x 11)	ECA-1VM100	Panasonic
4	2	C6 C7	100 µF, 10 V, Electrolytic, Low ESR, 500 mΩ, (5 x 11.5)	ELXZ100ELL101MEB5D	Nippon Chemi-Con
5	1	C8	220 µF, 25 V, Electrolytic, Very Low ESR, 72 mΩ, (8 x 11.5)	EKZE250ELL221MHB5D	Nippon Chemi-Con
6	1	C9	1.5 µF, 25V, Ceramic, X7R, 0805	C2012X7R1E155M125AC	TDK
7	1	D1	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
8	2	D2 D3	600 V, 1 A, Ultrafast Recovery, 30 ns, SOD57	BYV26C	Philips
9	1	D4	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
10	1	L1	470 µH, 0.3 A, 5.5 x 10.5 mm	SBC1-471-301	Tokin
11	1	R1	19.1 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1912V	Panasonic
12	1	R2	2.55 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2551V	Panasonic
13	1	R3	5.9 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF5901V	Panasonic
14	1	R4	43 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ433V	Panasonic
15	1	RF1	8.2 Ω, 1 W, 5% , Fusible/Flame Proof Wire Wound	FKN1WSJR-52-8R2	Yageo
16	1	T1	Bobbin, EE10, Vertical, 8 pins (10.2 mm W x 10.4 mm L x 9.7 mm H)	EE-1016	Yulongxin
17	3	TP1 TP4 TP6	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
18	1	TP2	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
19	2	TP3 TP5	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
20	1	U1	LinkSwitch-TN2, SO-8C	LNK3206D	Power Integrations
21	1	U2	5 V, 100 mA, Regulator, 5%, 0 to 125C, TO-92	LM78L05ACZ	National Semi

7 Transformer Specification

7.1 Electrical Diagram

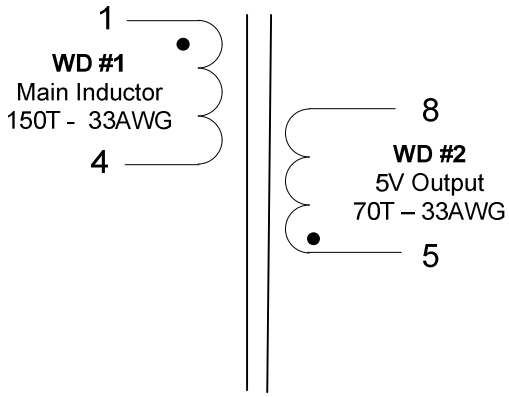

Figure 6 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Main Inductance	Pin 4 and pin 1 together, measured at 80 kHz, 0.4 V_{RMS}.	1200 µH ±10%
Resonant Frequency	Pin 4 and pin 1 are shorted together with all other windings open.	1.1 MHz
Electrical Strength	1 second, 60 Hz, from primary to secondary.	N/A

7.3 Material List

Item	Description
[1]	Core: PC44, Gapped.
[2]	Bobbin: Vertical 8 Pin, EE10.
[3]	Magnet Wire: #33 AWG.
[4]	Tape, 3M 1298 Polyester Film, 2.0 Mils Thick, 7.0 mm Wide.
[5]	Varnish Dolph BC-359 or Equivalent.

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7.4 Transformer Build Diagram

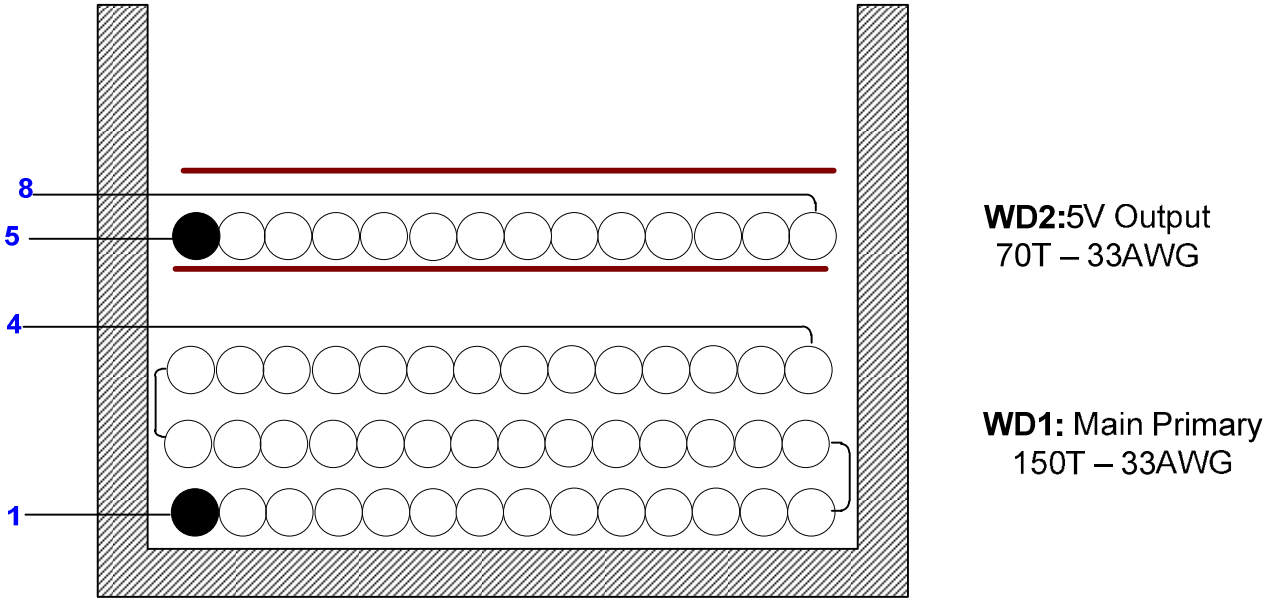
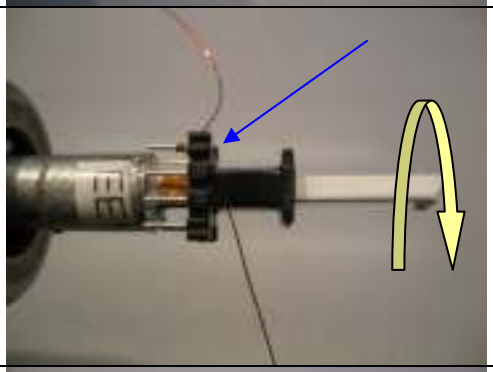


Figure 7 – Transformer Build Diagram.

7.5 Transformer Instructions

General Note	For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side (see illustration). Winding direction as shown is counter-clockwise.
WD1	Starting at pin 1, wind 150 turns of wire item [3] in five layers. Finish at pin 4.
Tape	Use 1 layer of tape item [4] for insulation.
WD2	Starting at pin 5, wind 70 turns of wire item [3] in three layers. Finish at pin 8. Spread last layer evenly across bobbin.
Tape	Use 1 layer of tape item [4] for insulation.
Assembly	Grind core halves for specified primary inductance, insert bobbin, and secure core halves.
Varnish	Dip varnish with item [5].
General Note	For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side (see illustration). Winding direction as shown is counter-clockwise.

7.6 Transformer Winding Illustrations

General Note		For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side (see illustration). Winding direction as shown is counter-clockwise.
WD 1		Starting at pin 1, wind 150 turns of wire item [3] in five layers.
Tape	 	Finish at pin 4. Apply one layer of tape item [4] for insulation.

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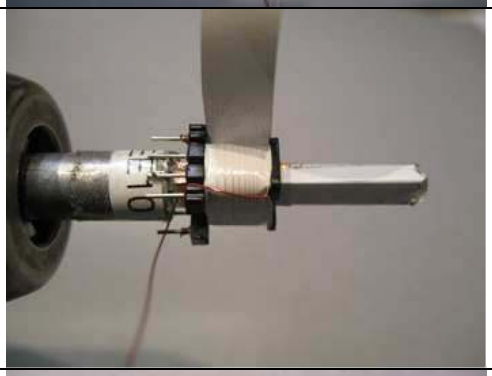
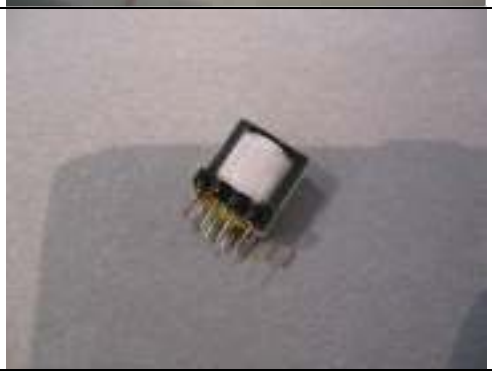
WD 2		Starting at pin 5, wind 70 turns of wire item [3] in three layers, spread last layer evenly across bobbin.
Tape		Finish at pin 8. Use 1 layer of tape item [4] for insulation.
Assembly		Grind core halves for specified primary inductance, insert bobbin, and secure core halves. Dip varnish.

8 Transformer Design Spreadsheet

Note: *Since the spreadsheet input is limited to a single value for voltage and current and this is a dual output design, the current specification was changed to 300 mA to account for the total combined power of both the 18 V and 5 V outputs.*

ACDC_LinkSwitchTN2-Buck_071816; Rev.0.1; Copyright Power Integrations 2016	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitchTN2 Buck
ENTER APPLICATION VARIABLES					
LINE VOLTAGE RANGE			Universal		AC line voltage range
VACMIN	85.00		85.00	volts AC	Minimum AC line voltage
VACTYP			115.00	volts AC	Typical AC line voltage
VACMAX	265.00		265.00	volts AC	Maximum AC line voltage
fL	50.00		50.00	Hz	AC mains frequency
LINE RECTIFICATION TYPE	H		H		Select 'F'ull wave rectification or 'H'alf wave rectification
VOUT	18.00		18.00	volts DC	Output voltage
IOUT	0.300		0.300	A	Average output current
EFFICIENCY	0.80		0.80		Efficiency estimate at output terminals
POUT			5.40	W	Continuous Output Power
CIN	24.00		24.00	uF	Input capacitor
VMIN			69.9	volts DC	Valley of the rectified input voltage
ENTER LINKSWITCH-TN2 VARIABLES					
OPERATION MODE			MCM		Mostly continuous mode of operation
CURRENT LIMIT MODE	STD		STD		Choose 'RED' for reduced current limit or 'STD' for standard current limit
PACKAGE	SO-8C		SO-8C		Select the device package
DEVICE SERIES	LNK32X6		LNK32X6		Generic LinkSwitch-TN2 device
DEVICE CODE			LNK3206		Required LinkSwitch-TN2 device
ILIMITMIN			0.450	A	Minimum current limit of the device
ILIMITTYP			0.482	A	Typical current limit of the device
ILIMITMAX			0.515	A	Maximum current limit of the device
RDSON			12.90	ohms	MOSFET's on-time drain to source resistance at 100degC
FSMIN			62000	Hz	Minimum switching frequency
FSTYP			68000	Hz	Typical switching frequency
FSMAX			72000	Hz	Maximum switching frequency
VDSON			2.00	volts DC	MOSFET on-time drain to source voltage estimate
DUTY			0.27		Maximum duty cycle
TIME_ON			4.398	us	MOSFET conduction time at the minimum line voltage
TIME_ON_MIN			1.379	us	MOSFET conduction time at the maximum line voltage
IRMS_MOSFET			0.163	A	MOSFET RMS current
BUCK INDUCTOR PARAMETERS					
INDUCTANCE_MIN			1080	uH	Minimum design inductance required for power delivery
INDUCTANCE_TYP	1200		1200	uH	Typical design inductance required for power delivery
INDUCTANCE_MAX			1320	uH	Maximum design inductance required for power delivery
TOLERANCE_INDUCTANCE			10	%	Tolerance of the design inductance
FACTOR_LOSS			0.85		Factor that accounts for "off-state" power loss to be supplied by inductor
IRMS_INDUCTOR			0.312	A	Inductor RMS current
FREEWHEELING DIODE PARAMETERS					
VF_FREEWHEELING			0.70	volts DC	Forward voltage drop of the freewheeling diode
PIV			600	volts DC	Peak inverse voltage rating of the freewheeling diode
IRMS_DIODE			0.266	A	Diode RMS current
TRR			<35	ns	Required reverse recovery time of the selected diode
BIAS/FEEDBACK PARAMETERS					
VF_BIAS			0.70	volts DC	Forward voltage drop of the bias diode

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RBIAS			2490	Ohms	Bias resistor
RBP			0.1	uF	BP pin capacitor
RFB			18700	Ohms	Feedback resistor
CFB			10	uF	Feedback capacitor
C_SOFTSTART			1-10	uF	If the output voltage is greater than 12 V or total output and system capacitance is greater than 100 uF, a soft start capacitor between 1uF and 10 uF is recommended

9 Performance Data

9.1 Full Load Efficiency vs. Input Line Voltage

9.1.1 Efficiency vs. Line Voltage, 4.5 W (250 mA on 18 V, No-Load on 5 V) and 4.75 W (250 mA on 18 V, Full Load on 5 V)

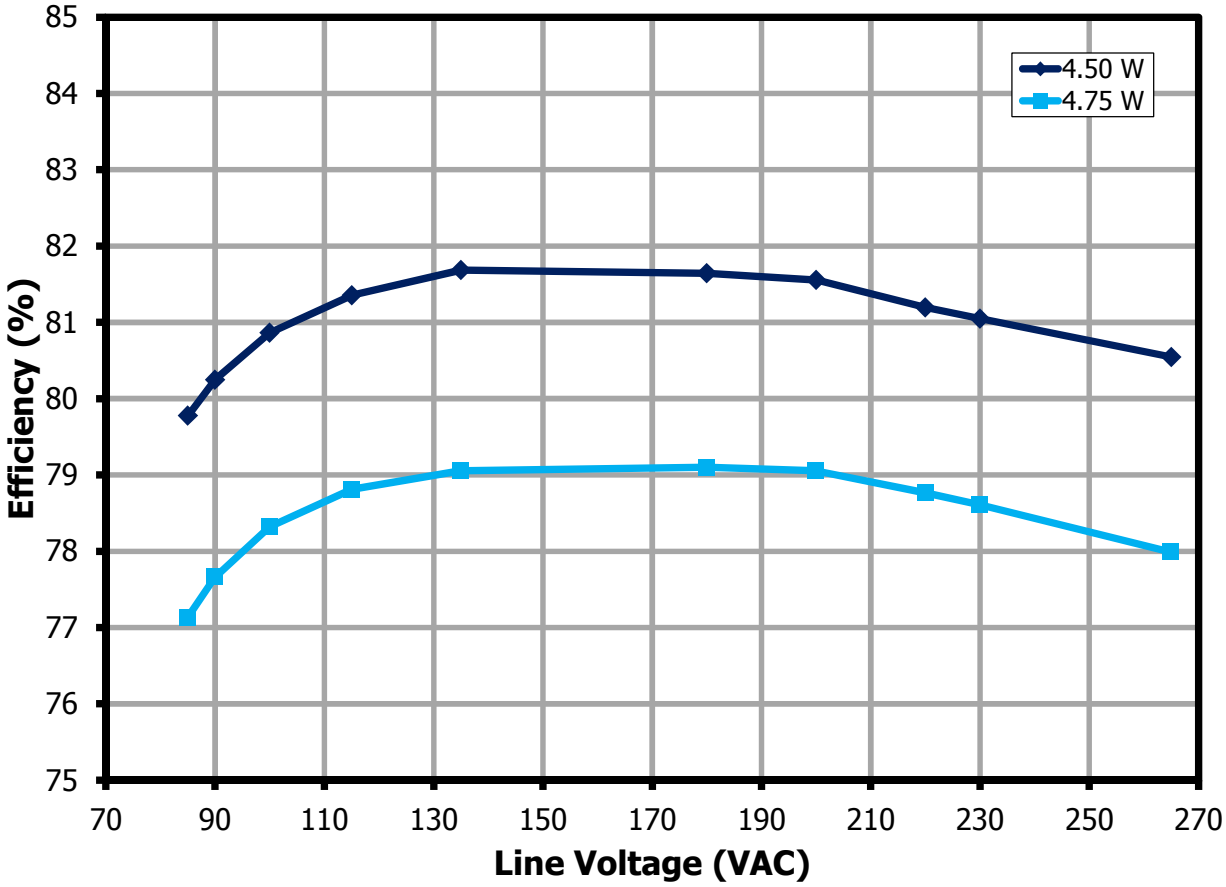

Figure 8 – Efficiency vs. Line Voltage, Room Temperature.

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9.2 Efficiency vs. Load

9.2.1 Efficiency at 18 V Output (25-250 mA on 18 V, No-Load on 5 V)

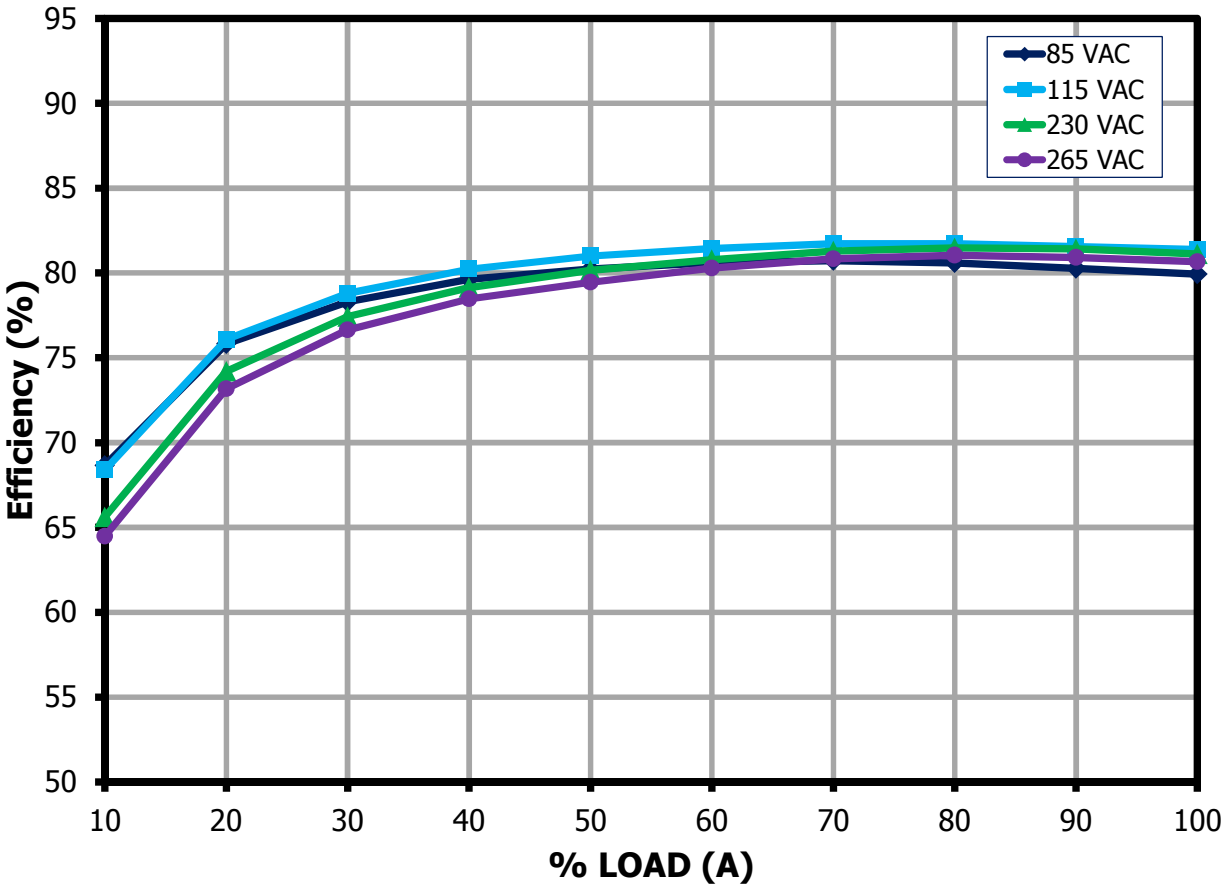

Figure 9 – Efficiency vs. Load, Room Ambient (measured at the Output Terminal).

9.2.2 Efficiency at 18 V Output (25-250 mA on 18 V, Full Load on 5 V)

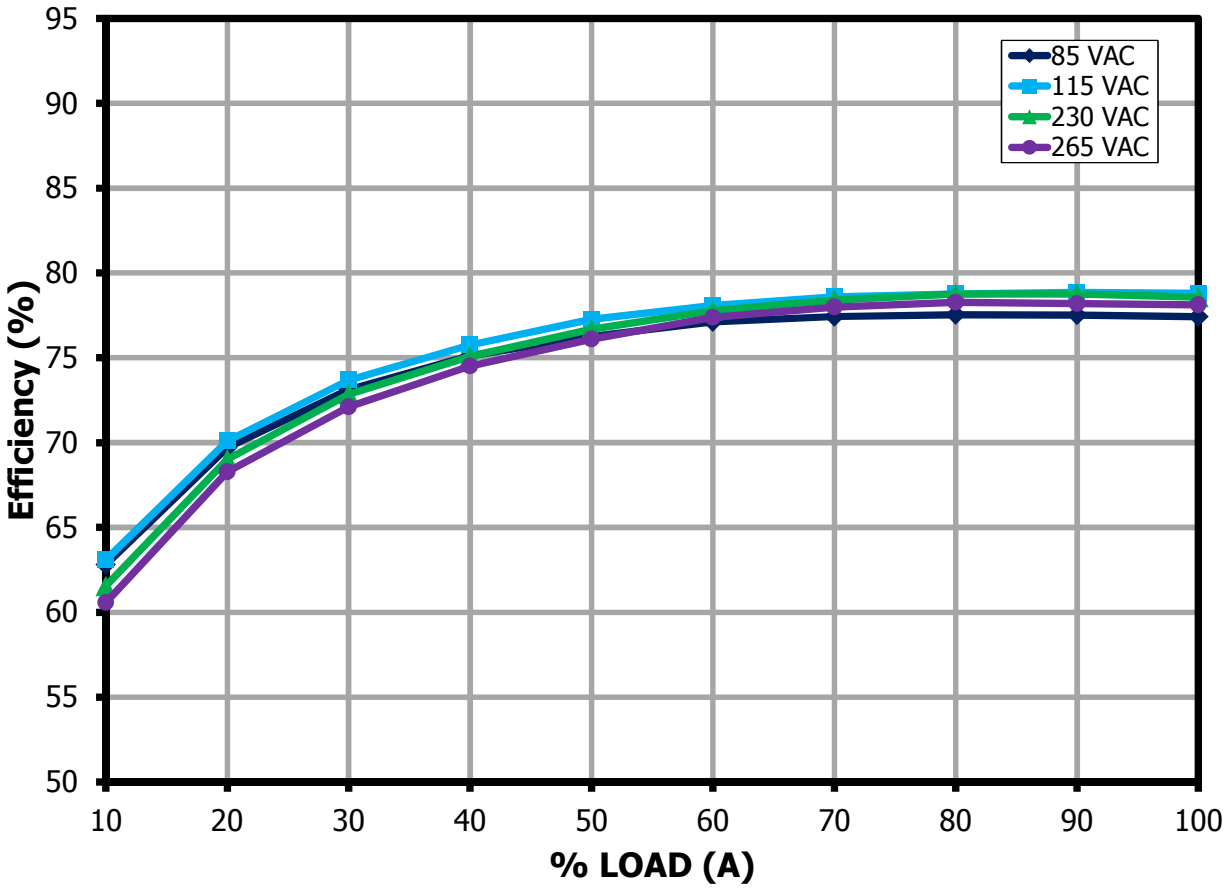

Figure 10 – Efficiency vs. Load, Room Ambient (Measured at the Output Terminal).

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9.3 No-Load Input Power

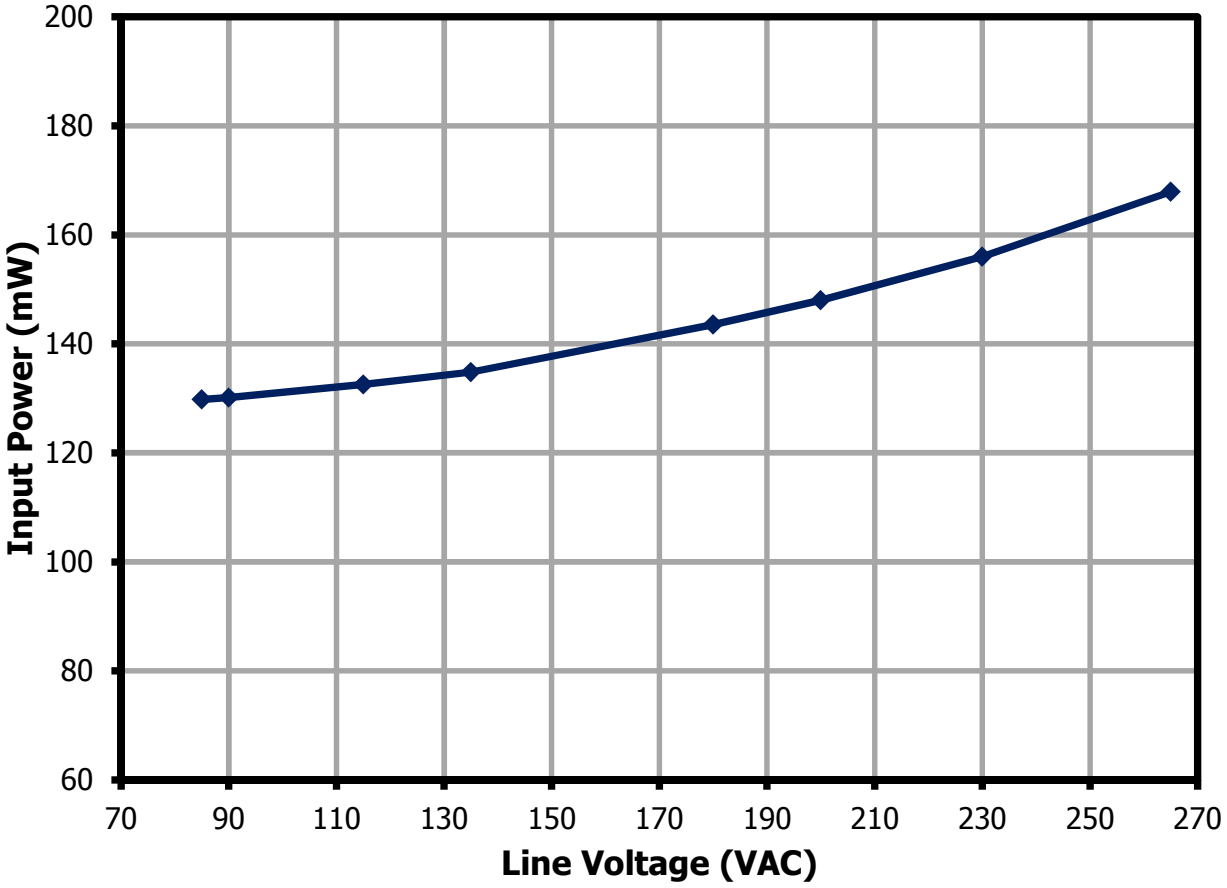

Figure 11 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

9.4 Line and Load Regulation

9.4.1 18 V Line Regulation at 4.5 W (250 mA on 18 V, No-Load on 5 V)

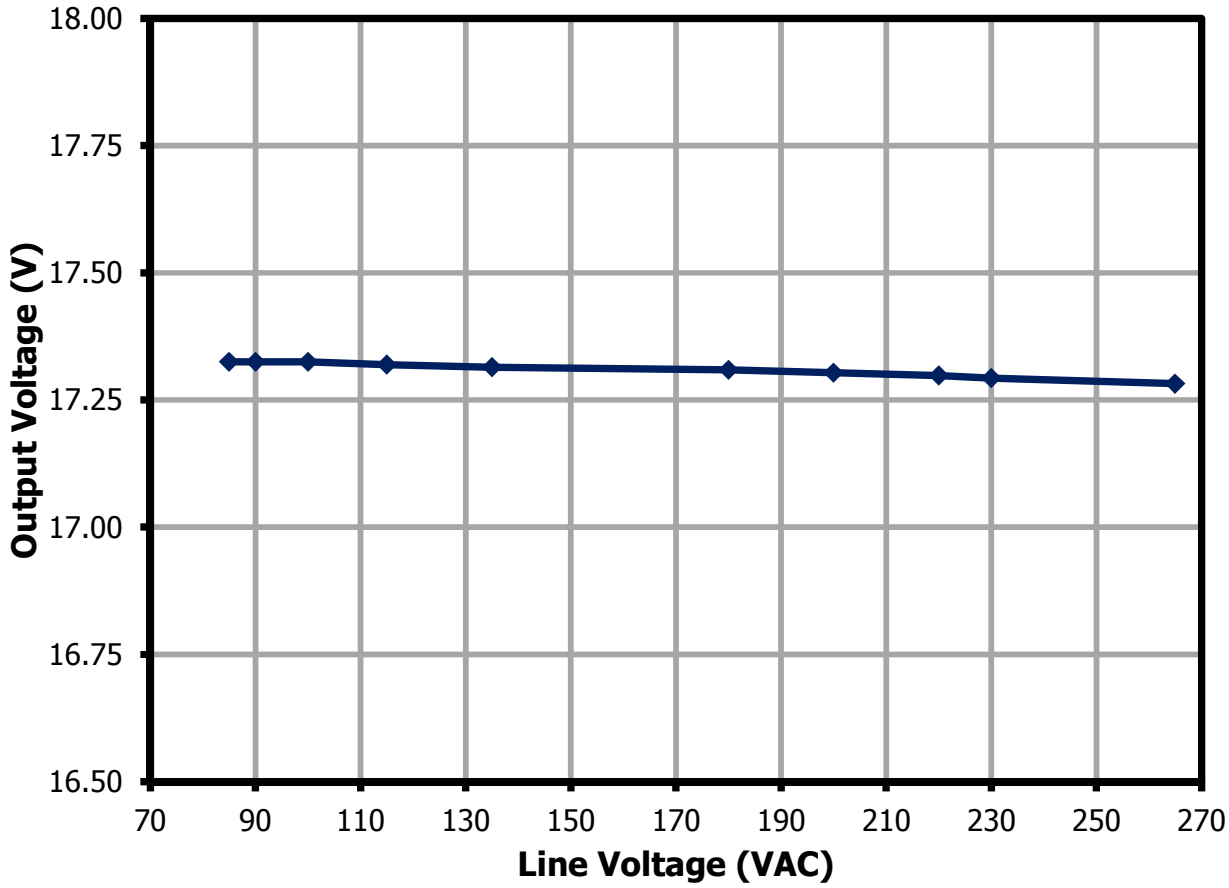

Figure 12 – Output Voltage vs. Input Line Voltage, Room Temperature.

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9.4.2 18 V Line Regulation at 4.75 W (250 mA on 18 V, Full Load on 5 V)

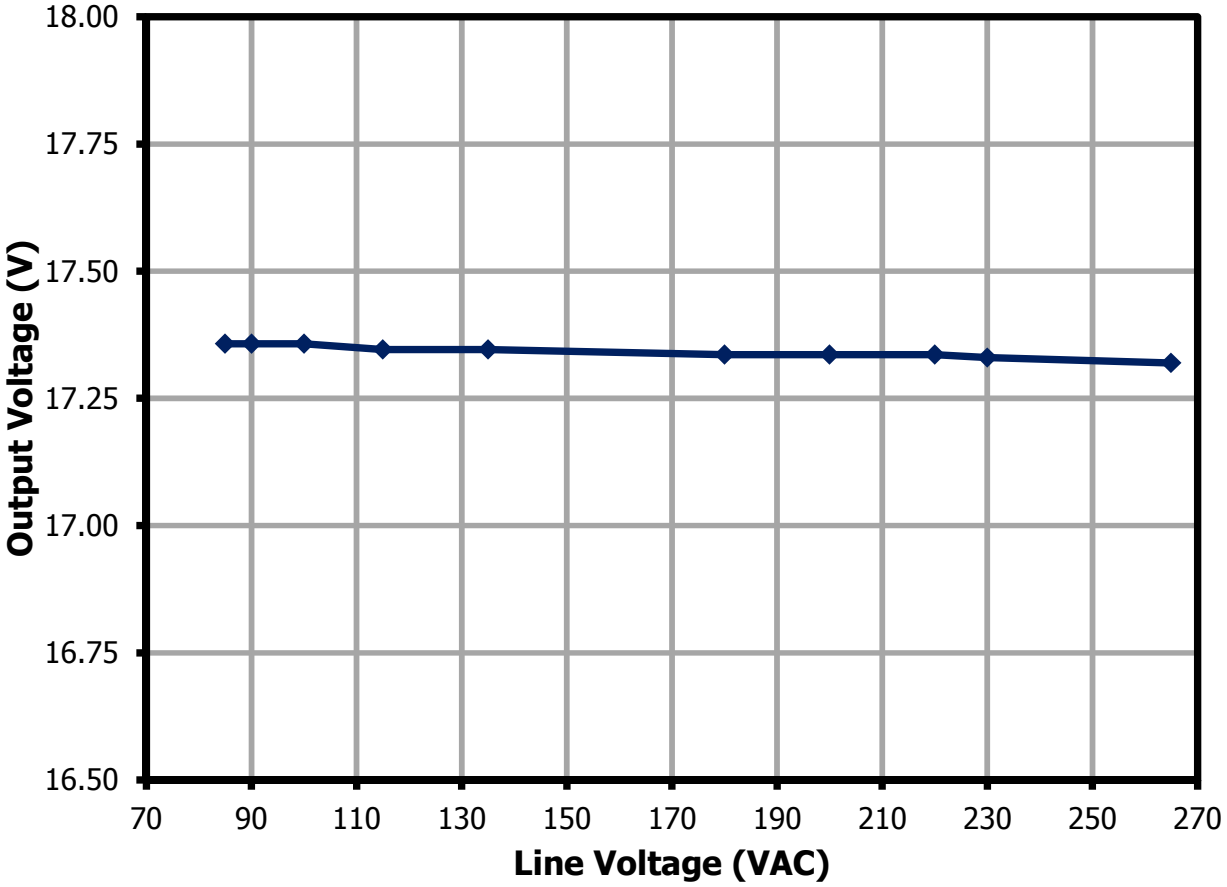

Figure 13 – Output Voltage vs. Input Line Voltage, Room Temperature.

9.4.3 18 V Load Regulation (25-250 mA on 18 V, No-Load on 5 V)

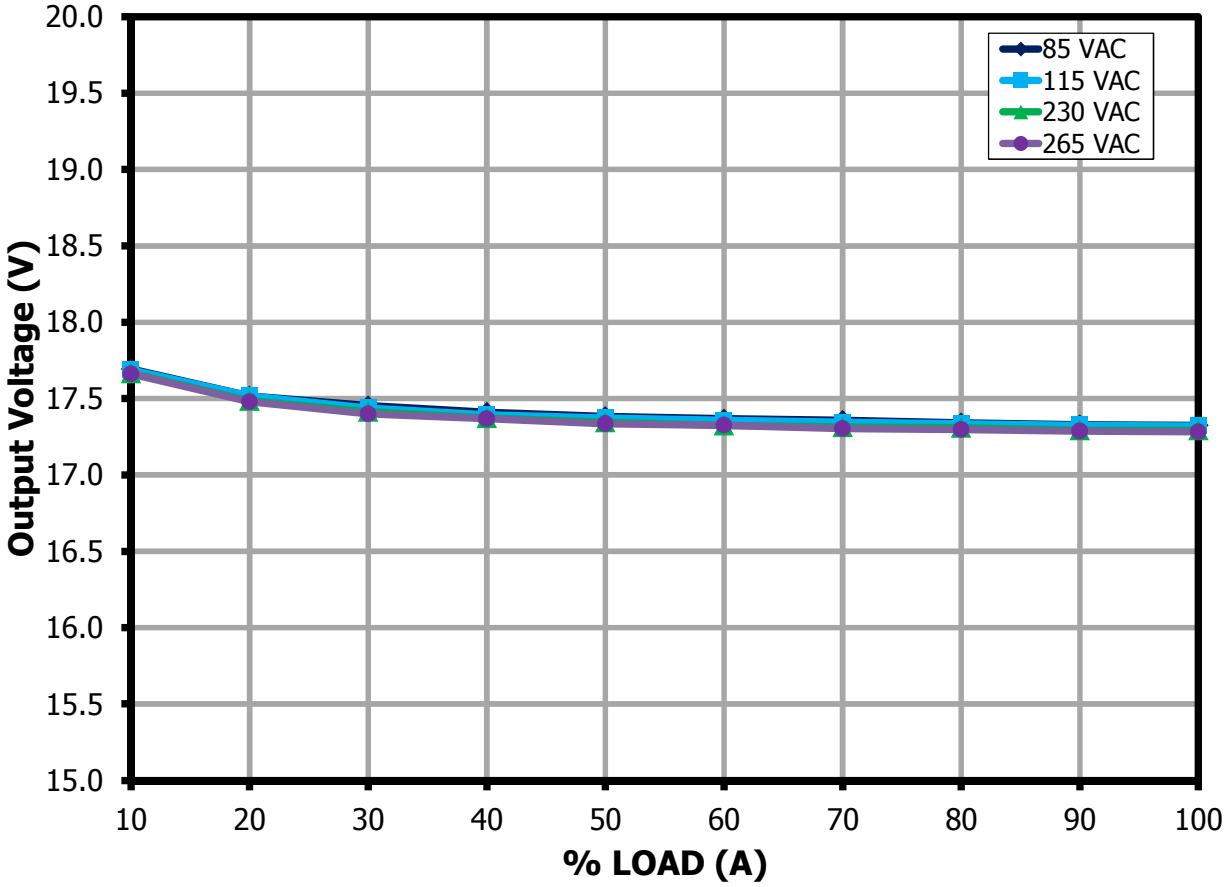

Figure 14 – Output Voltage vs. Output Load, Room Temperature.

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9.4.4 18 V Load Regulation (25-250 mA on 18 V, Full Load on 5 V)

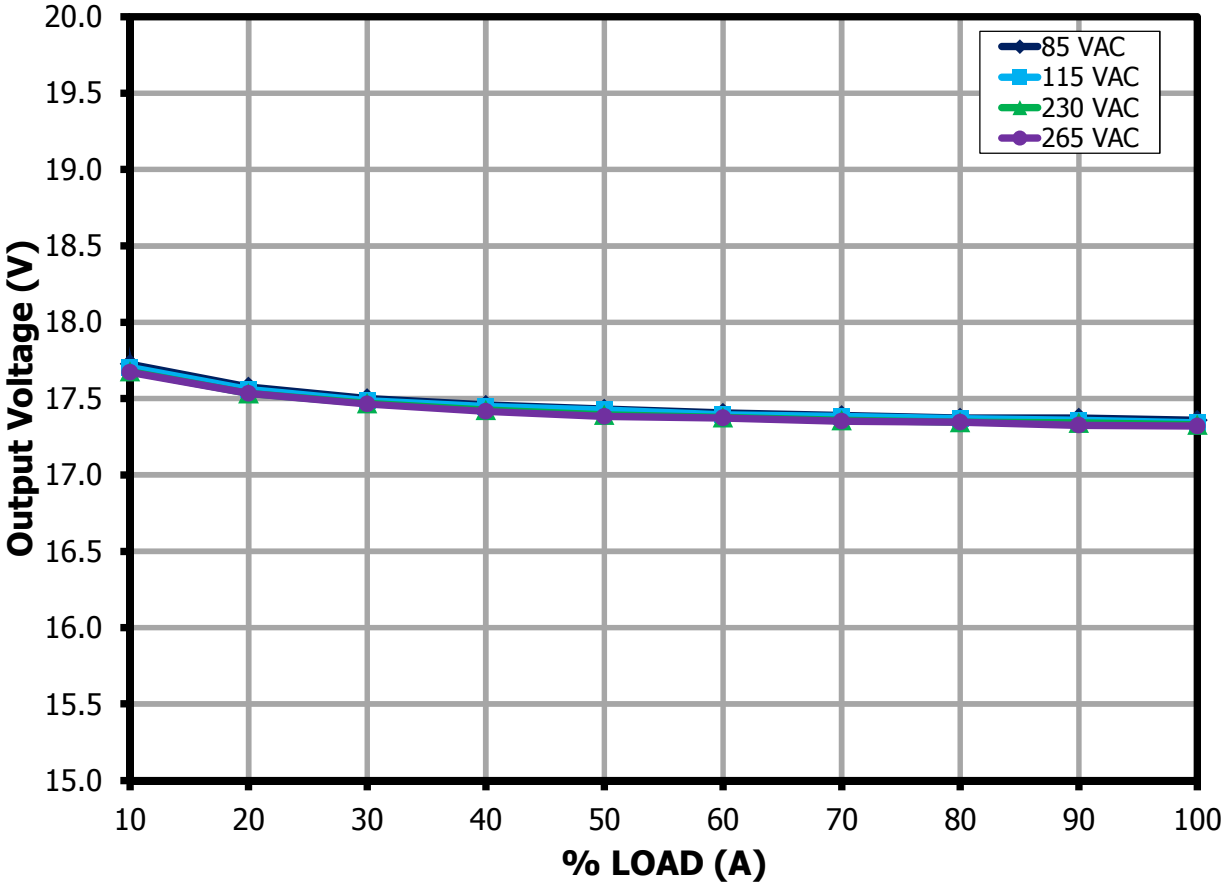


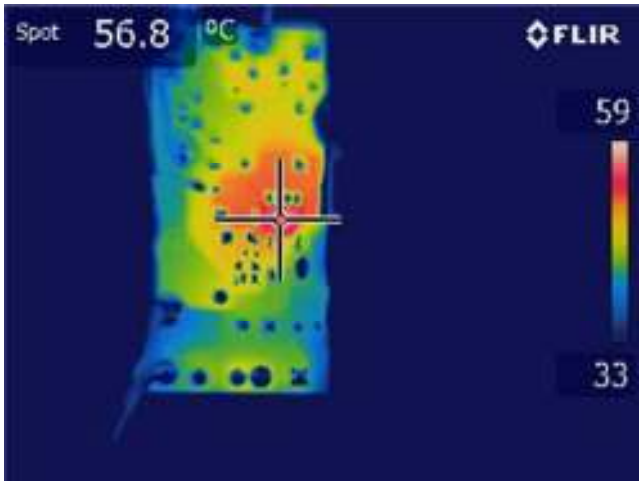
Figure 15 – Output Voltage vs. Output Load, Room Temperature.

10 Thermal Performance

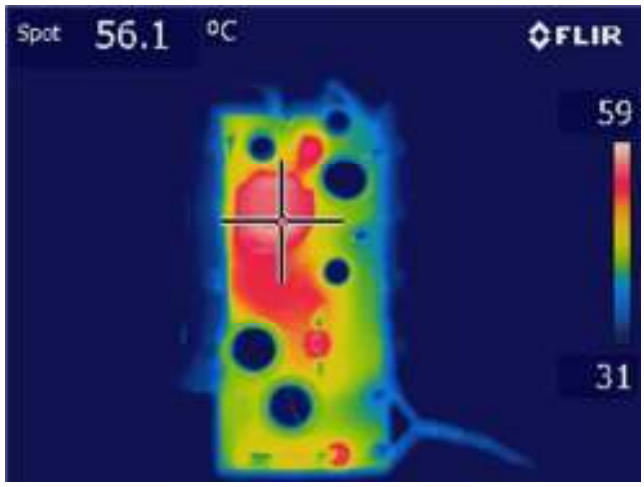
10.1 Open Case

For thermal measurement, soak the power supply first for 2 hours. It is recommended that the power supply be placed in an enclosure box to ensure that the ambient temperature is within the room temperature. Add a thermocouple to monitor ambient temperature.

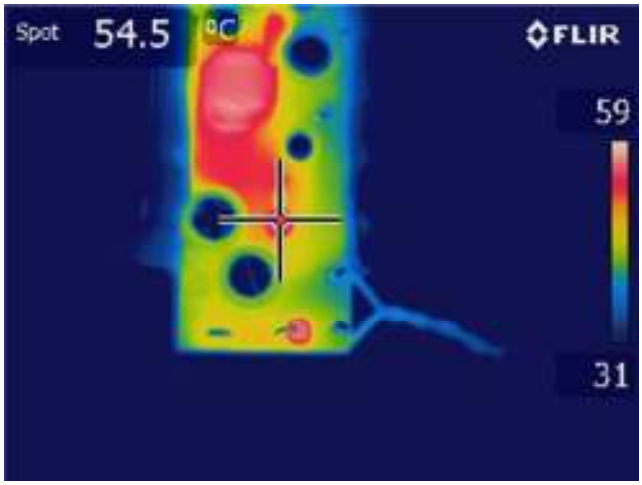
10.1.1 85 VAC at Room Temperature



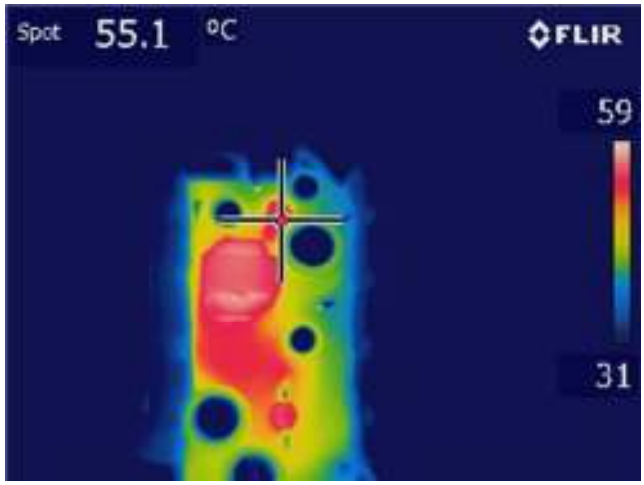
U1 – LinkSwitch-TN2.
Spot Temperature – 56.8 °C.



T1 – Transformer.
Spot Temperature – 56.1 °C.



D2 – Free Wheel Diode.
Spot Temperature – 54.5 °C.



U2 – Linear Regulator.
Spot Temperature – 55.1 °C.

Figure 16 – Measured Temperature at 4.75 W with an Ambient Temperature of 27.1 °C.

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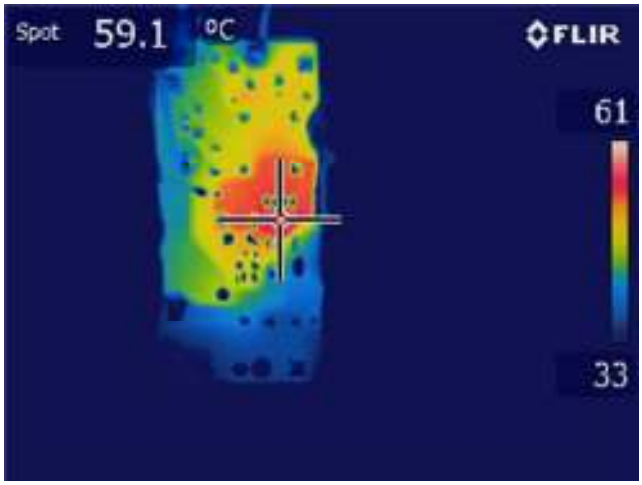
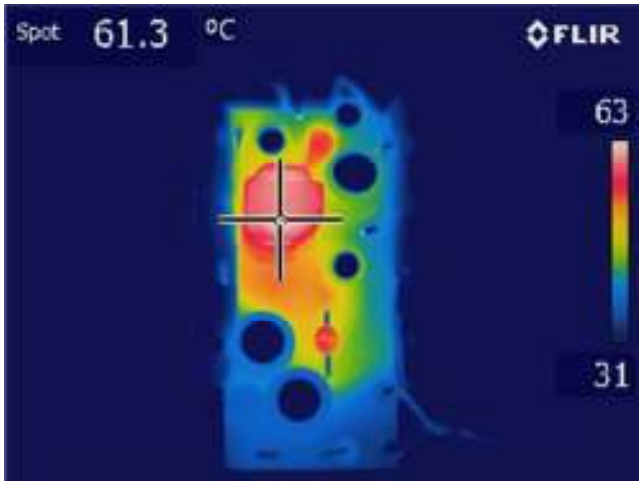
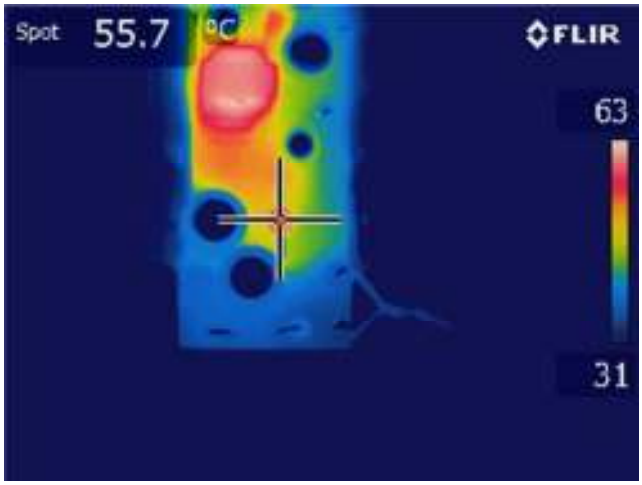
10.1.2 265 VAC at Room Temperature



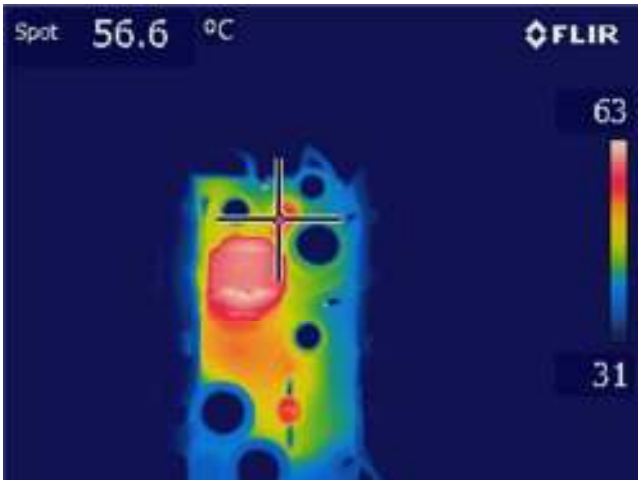
U1 – LinkSwitch-TN2.
Spot Temperature – 59.1 °C.



T1 – Transformer.
Spot Temperature – 61.3 °C.



D2 – Free Wheel Diode.
Spot Temperature – 55.7 °C.



U2 – Linear Regulator.
Spot Temperature – 56.6 °C.

Figure 17 – Measured Temperature at 4.75 W with an Ambient Temperature of 27.7 °C

11 Waveforms

11.1 18 V Output Load Transient Response

Results were taken at the output terminal which is the typical specified measurement condition. The +5 V output is loaded with 50 mA (full load).

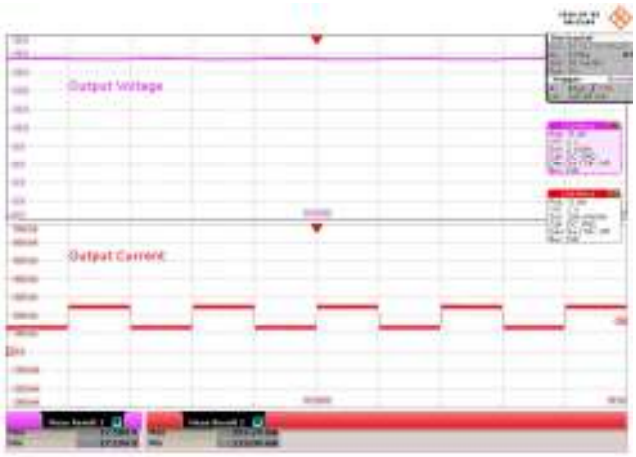


Figure 18 – 85 VAC, 50-100% Load Step.
V_{MAX}: 17.589 V.
V_{MIN}: 17.194 V.
Upper: V_{OUT}, 2 V / div.
Lower: I_{LOAD}, 100 mA / div., 10 ms / div.

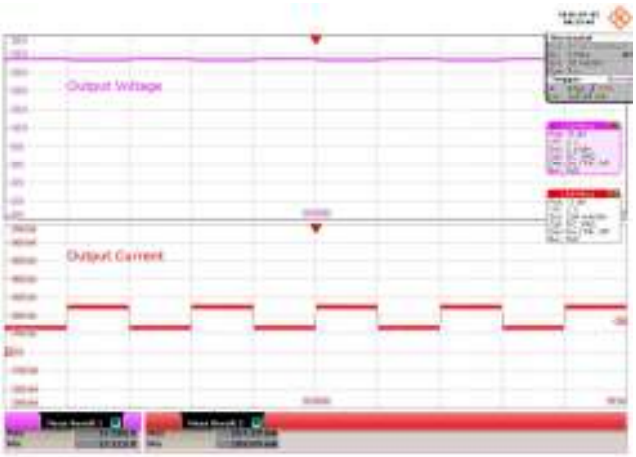


Figure 19 – 265 VAC, 50-100% Load Step.
V_{MAX}: 17.589 V.
V_{MIN}: 17.115 V.
Upper: V_{OUT}, 2 V / div.
Lower: I_{LOAD}, 100 mA / div., 10 ms / div.

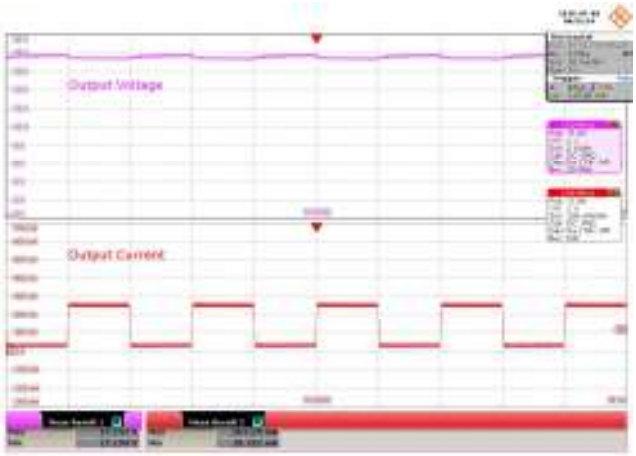


Figure 20 – 85 VAC, 10-100% Load Step.
V_{MAX}: 17.747 V.
V_{MIN}: 17.194 V.
Upper: V_{OUT}, 2 V / div.
Lower: I_{LOAD}, 100 mA / div., 10 ms / div.

Figure 21 – 265 VAC, 10-100% Load Step.
V_{MAX}: 17.747 V.
V_{MIN}: 17.194 V.
Upper: V_{OUT}, 2 V / div.
Lower: I_{LOAD}, 100 mA / div., 10 ms / div.

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11.2 Switching Waveforms

11.2.1 Drain to Source Voltage, Current, Free Wheel and Secondary Rectifier Diode Waveforms during Normal Operation.

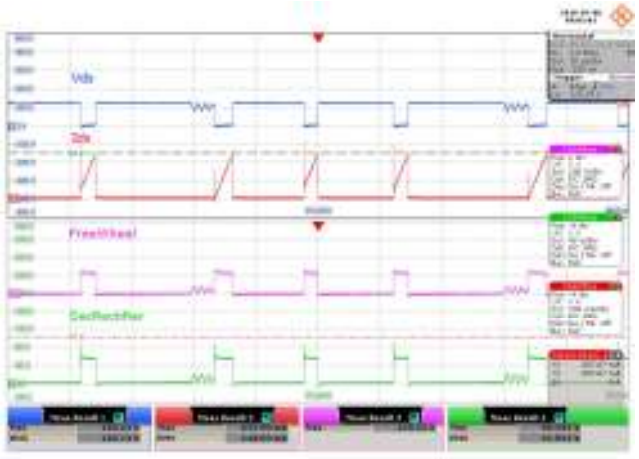

Figure 22 – 85 VAC Input.
Condition: 18 V – 250 mA, 5 V – 0 A.
Upper: V_{DRAIN}, 50 V / div.
Upper Middle: I_{DRAIN}, 200 mA / div.
Lower Middle: V_{FWL}, 100 V / div.
Lower: V_{SECREC}, 40 V / div., 20 µs / div.

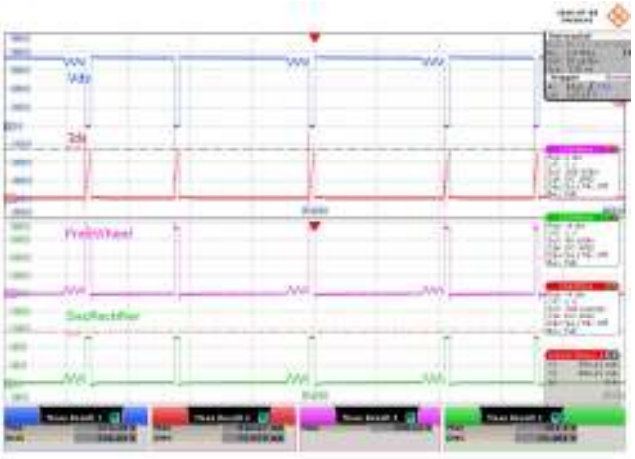

Figure 23 – 265 VAC Input.
Condition: 18 V – 250 mA, 5 V – 0 A.
Upper: V_{DRAIN}, 50 V / div.
Upper Middle: I_{DRAIN}, 200 mA / div.
Lower Middle: V_{FWL}, 100 V / div.
Lower: V_{SECREC}, 40 V / div., 20 µs / div.

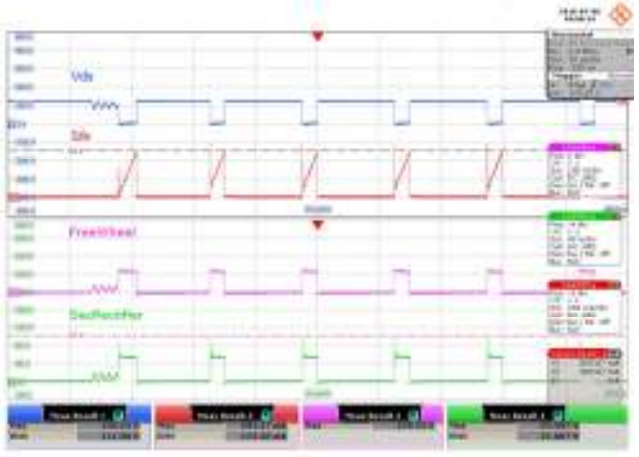

Figure 24 – 85 VAC Input.
Condition: 18 V – 250 mA, 5 V – 50 mA.
Upper: V_{DRAIN}, 50 V / div.
Upper Middle: I_{DRAIN}, 200 mA / div.
Lower Middle: V_{FWL}, 100 V / div.
Lower: V_{SECREC}, 40 V / div., 20 µs / div.

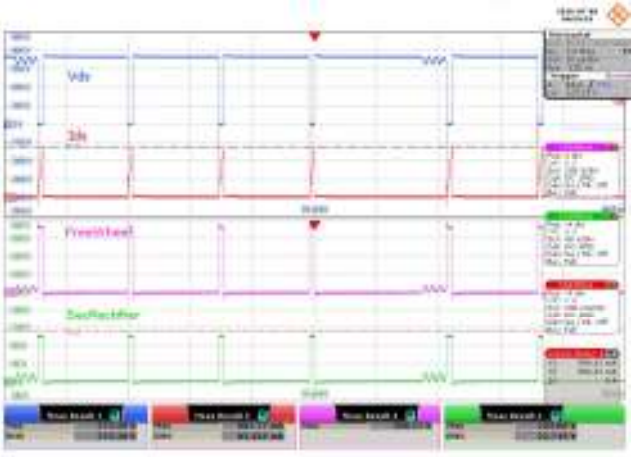

Figure 25 – 265 VAC Input.
Condition: 18 V – 250 mA, 5 V – 50 mA.
Upper: V_{DRAIN}, 50 V / div.
Upper Middle: I_{DRAIN}, 200 mA / div.
Lower Middle: V_{FWL}, 100 V / div.
Lower: V_{SECREC}, 40 V / div., 20 µs / div.

11.2.2 Drain to Source Voltage and Current Waveforms during Start-up

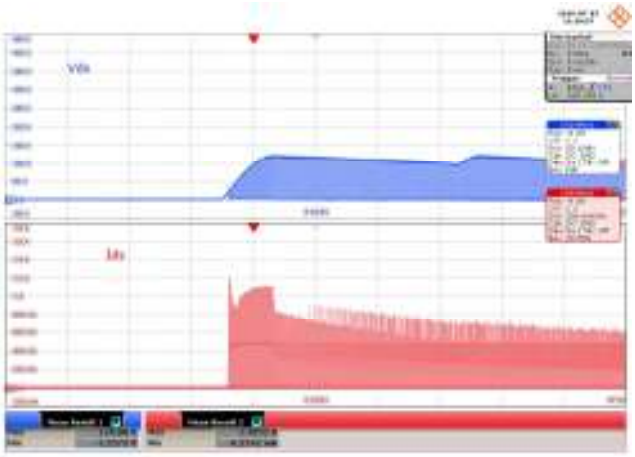

Figure 26 – 85 VAC Input.
Condition: 18 V – 250 mA, 5 V – 0 A.
Upper: V_{DRAIN}, 50 V, 5 ms / div.
Lower: I_{DRAIN}, 200 mA / div.

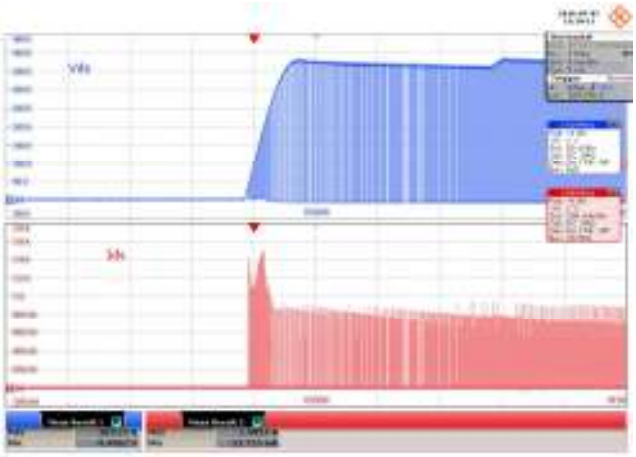

Figure 27 – 265 VAC Input.
Condition: 18 V – 250 mA, 5 V – 0 A.
Upper: V_{DRAIN}, 50 V, 5 ms / div.
Lower: I_{DRAIN}, 200 mA / div.

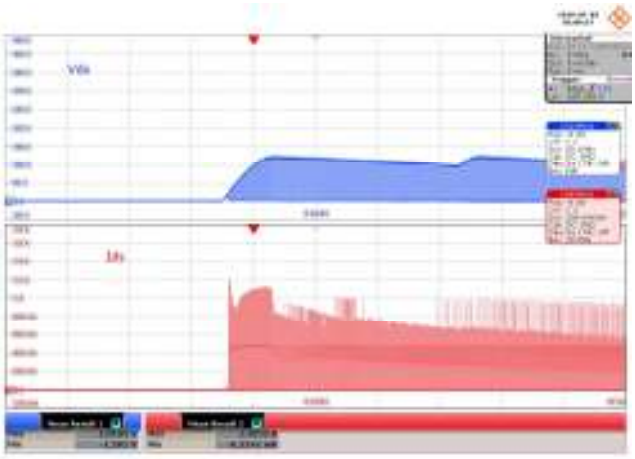

Figure 28 – 85 VAC Input.
Condition: 18 V – 250 mA, 5 V – 50 mA.
Upper: V_{DRAIN}, 50 V, 5 ms / div.
Lower: I_{DRAIN}, 200 mA / div.

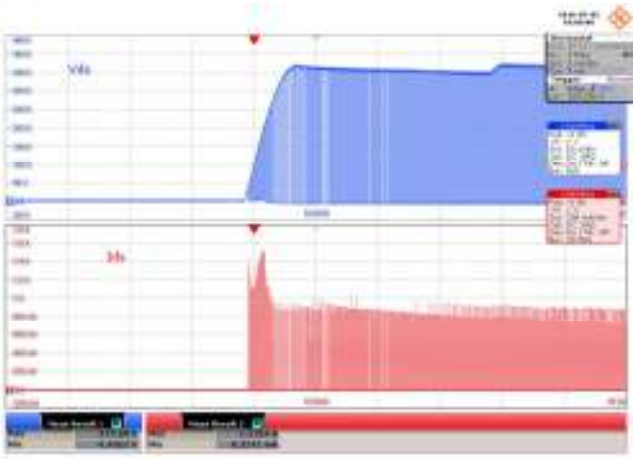

Figure 29 – 265 VAC Input.
Condition: 18 V – 250 mA, 5 V – 50 mA.
Upper: V_{DRAIN}, 50 V, 5 ms / div.
Lower: I_{DRAIN}, 200 mA / div.

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11.2.3 Input and Output Voltages Waveforms during Start-up

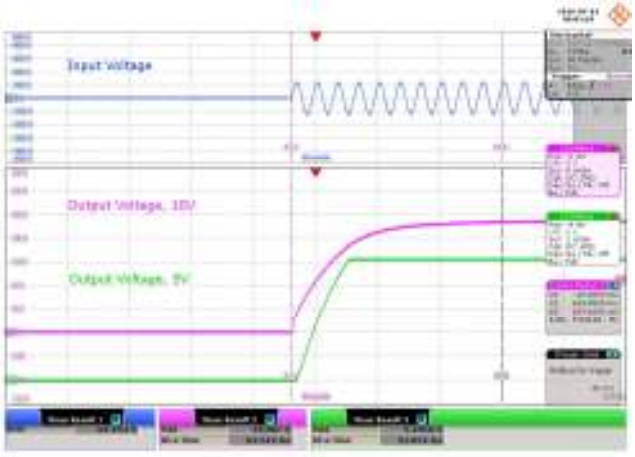

Figure 30 – 85 VAC Input.
Condition: 18 V – 0 A, 5 V – 0 A.
Upper: V_{IN}, 100 V, 50 ms / div.
Middle:V_{OUT1}, 4 V / div.
Lower: V_{OUT2}, 1 V / div.

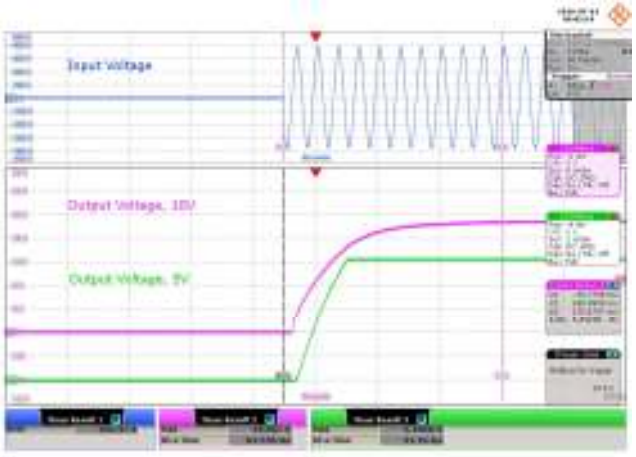

Figure 31 – 265 VAC Input.
Condition: 18 V – 0 A, 5 V – 0 A.
Upper: V_{IN}, 100 V, 50 ms / div.
Middle:V_{OUT1}, 4 V / div.
Lower: V_{OUT2}, 1 V / div.

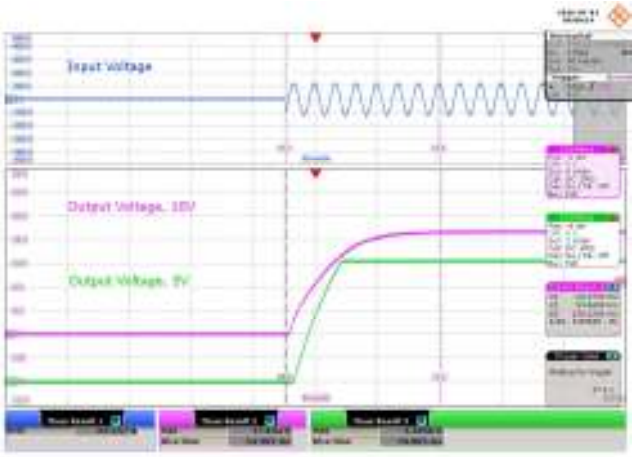

Figure 32 – 85 VAC Input
Condition: 18 V – 250 mA, 5 V – 0 A.
Upper: V_{IN}, 100 V, 50 ms / div.
Middle:V_{OUT1}, 4 V / div.
Lower: V_{OUT2}, 1 V / div.

Figure 33 – 265 VAC Input
Condition: 18 V – 250 mA, 5 V – 0 A.
Upper: V_{IN}, 100 V, 50 ms / div.
Middle:V_{OUT1}, 4 V / div.
Lower: V_{OUT2}, 1 V / div.

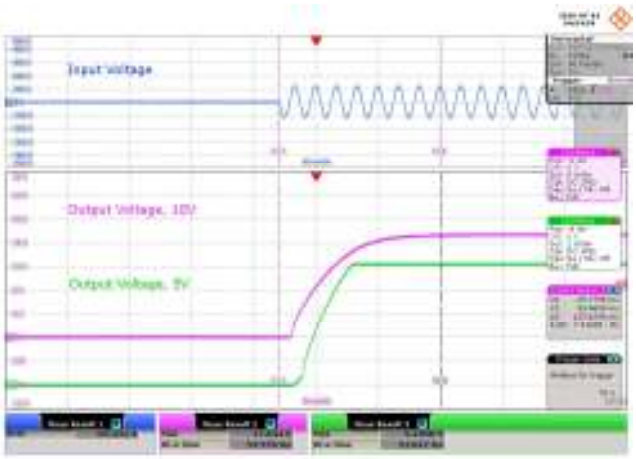

Figure 34 – 85 VAC Input.
Condition: 18 V – 250 mA, 5 V – 50 mA.
Upper: V_{IN}, 100 V, 50 ms / div.
Middle:V_{OUT1}, 4 V / div.
Lower: V_{OUT2}, 1 V / div.

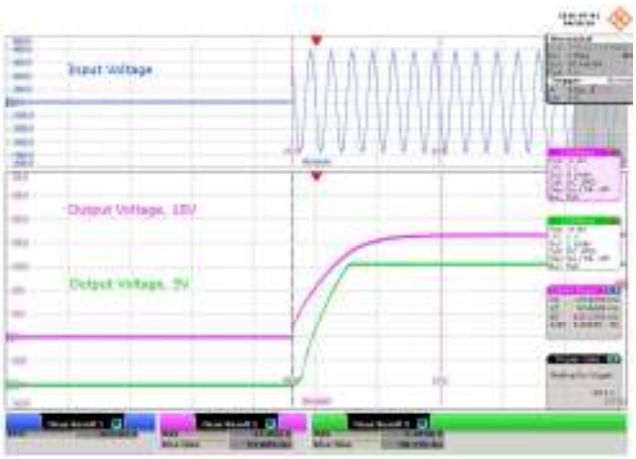

Figure 35 – 265 VAC Input.
Condition: 18 V – 250 mA, 5 V – 50 mA.
Upper: V_{IN}, 100 V, 50 ms / div.
Middle:V_{OUT1}, 4 V / div.
Lower: V_{OUT2}, 1 V / div.

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11.2.4 Output Short Auto-Restart

Short the main output (18V) and monitor V_{DS}, I_{DS}, output voltage and output current.

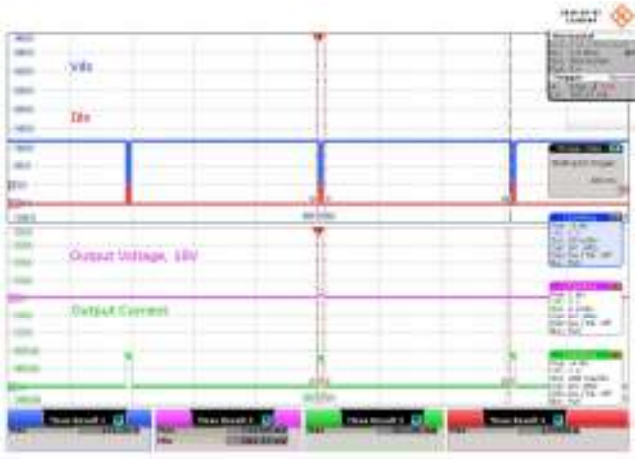

Figure 36 – 85 VAC Input.
Condition: 18 V – Shorted, 5 V – 50 mA.
Auto-Restart: 1.49 s.
Upper: V_{DS}, 50 V / div., 500 ms / div.
Upper Middle: I_{DS}, 500 mA / div.
Lower Middle: V_{OUT18}, 4 V / div.
Lower: I_{OUT18}, 400 mA / div.

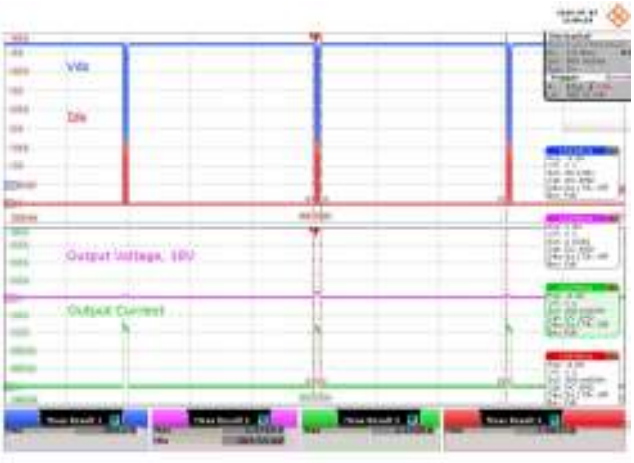

Figure 37 – 265 VAC Input.
Condition: 18 V – Shorted, 5 V – 50 mA.
Auto-Restart: 1.49 s.
Upper: V_{DS}, 50 V / div., 500 ms / div.
Upper Middle: I_{DS}, 500 mA / div.
Lower Middle: V_{OUT18}, 4 V / div.
Lower: I_{OUT18}, 400 mA / div.

11.3 Output Ripple Measurements

11.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

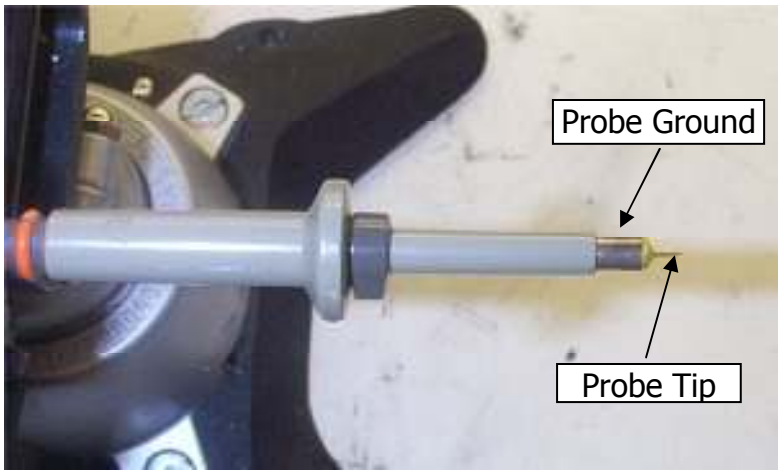

Figure 38 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

Figure 39 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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11.3.2 Measurement Results

11.3.3 Output Ripple Graph (0-250 mA on 18 V, No-Load on 5 V)

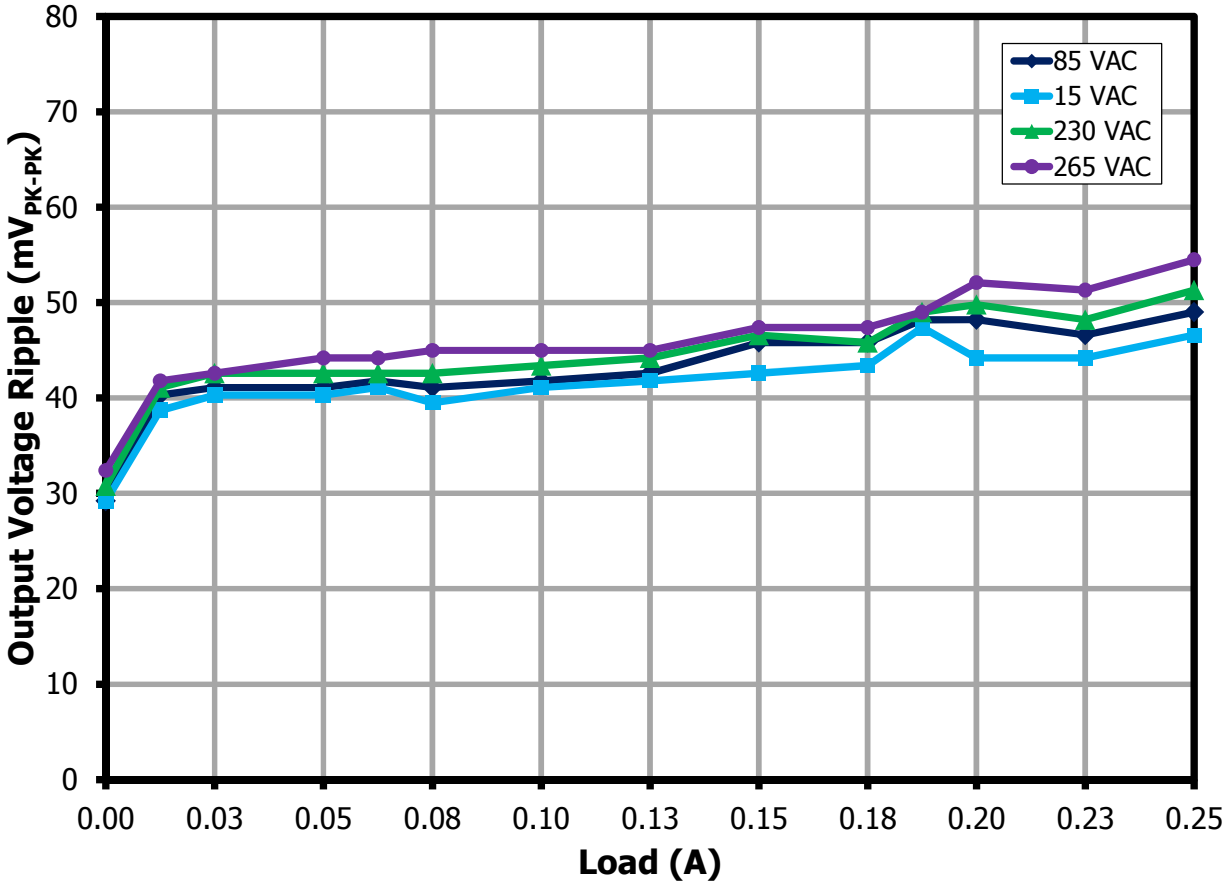

Figure 40 – Output Ripple Voltage at 4.50 W.

85 V RIPPLE (mV_{PK-PK})	115 V RIPPLE (mV_{PK-PK})	230 V RIPPLE (mV_{PK-PK})	265 V RIPPLE (mV_{PK-PK})
49.0	46.2	51.3	54.5

11.3.4 Output Ripple Graph (0-250 mA on 18 V, Full Load on 5 V)

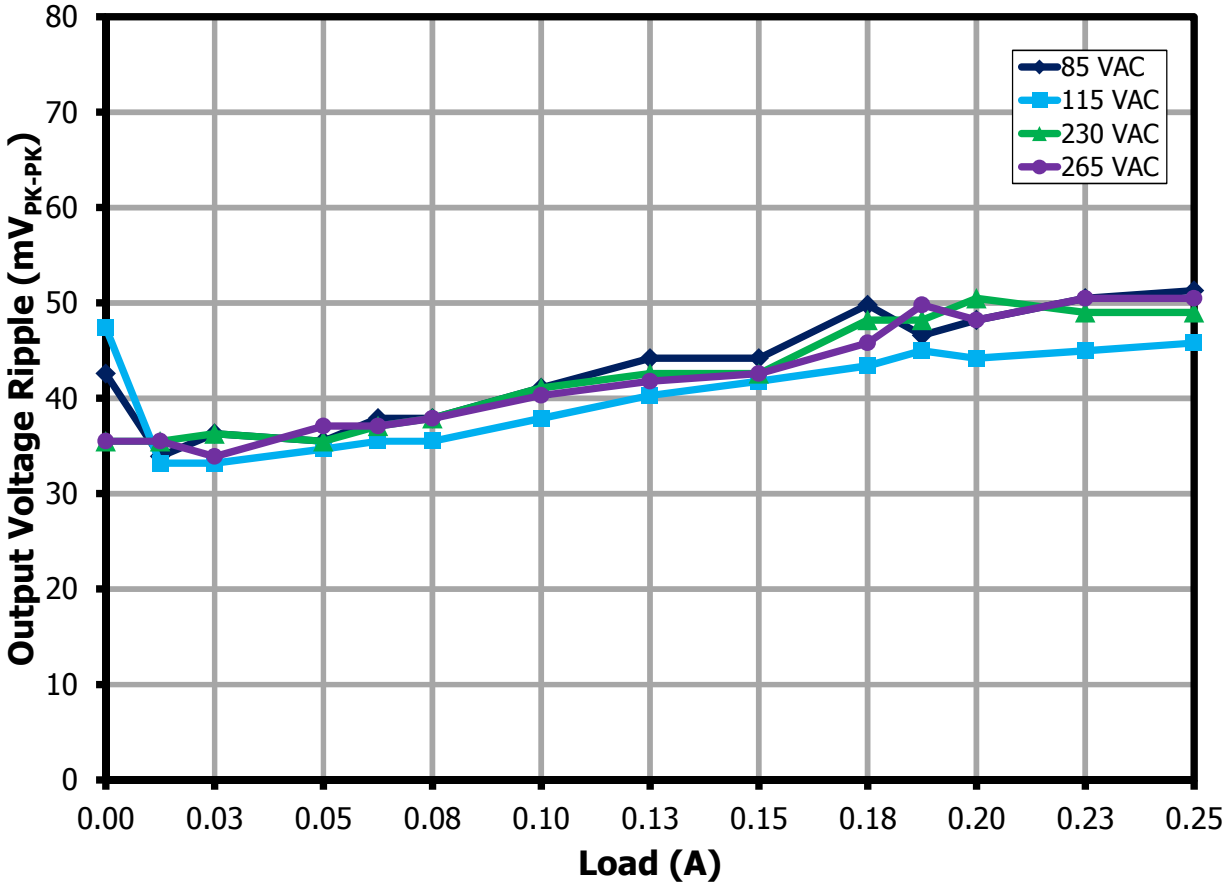

Figure 41 – Output Ripple Voltage at 4.75 W.

85 V RIPPLE (mV_{PK-PK})	115 V RIPPLE (mV_{PK-PK})	230 V RIPPLE (mV_{PK-PK})	265 V RIPPLE (mV_{PK-PK})
51.3	45.8	49.0	50.5

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11.3.5 Output Ripple Voltage Waveforms for 18 V Output

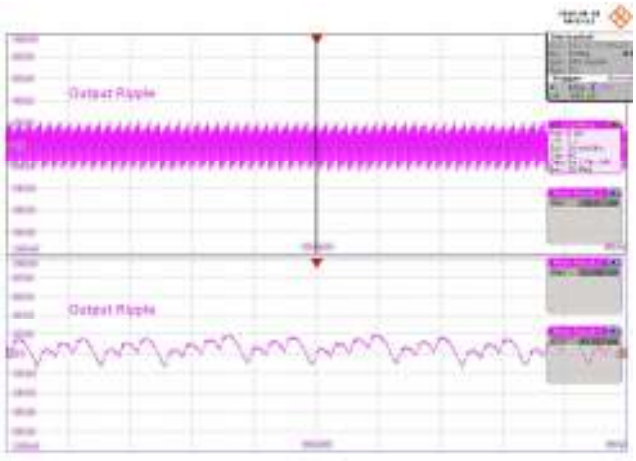

Figure 42 – 85 VAC Input.
Condition: 18 V – 250 mA, 5 V – 0 A.
V_{RIPPLE}, 20 mV / div., 100 ms, 100 µs / div.

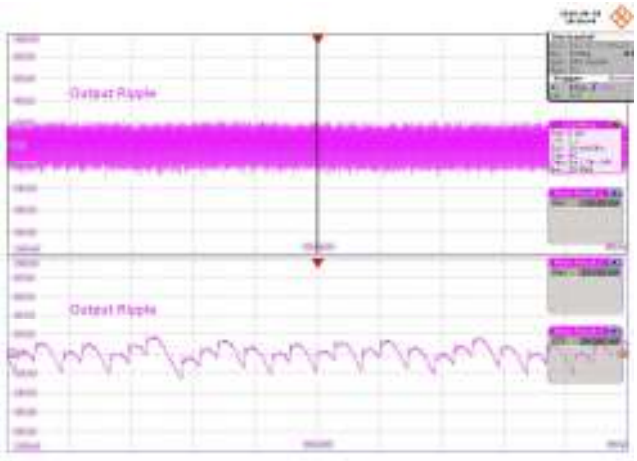

Figure 43 – 265 VAC Input.
Condition: 18 V – 250 mA, 5 V – 0 A.
V_{RIPPLE}, 20 mV / div., 100 ms, 100 µs / div.

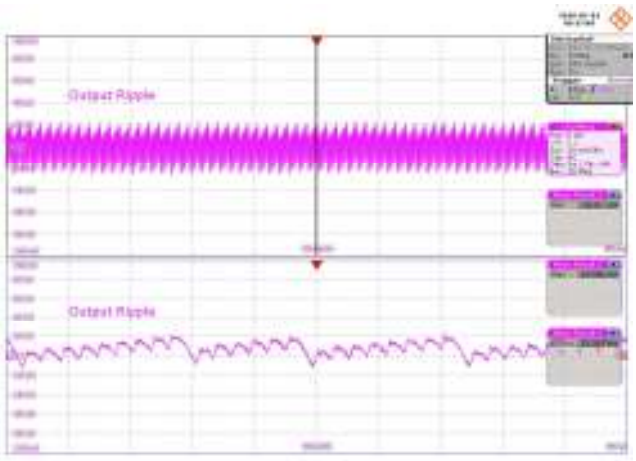

Figure 44 – 85 VAC Input.
Condition: 18 V – 250 mA, 5 V – 50 mA.
V_{RIPPLE}, 20 mV / div., 100 ms, 100 µs / div.

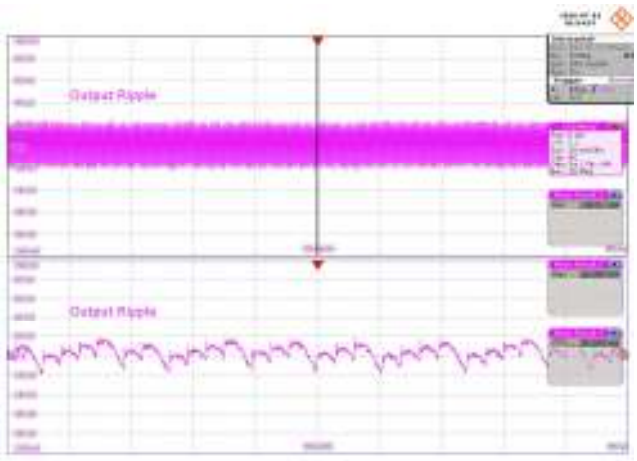

Figure 45 – 265 VAC Input.
Condition: 18 V – 250 mA, 5 V – 50 mA.
V_{RIPPLE}, 20 mV / div., 100 ms, 100 µs / div.

12 Conducted EMI

12.1 Test Setup Equipment

12.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power meter Hi-tester.
4. Chroma measurement test fixture.

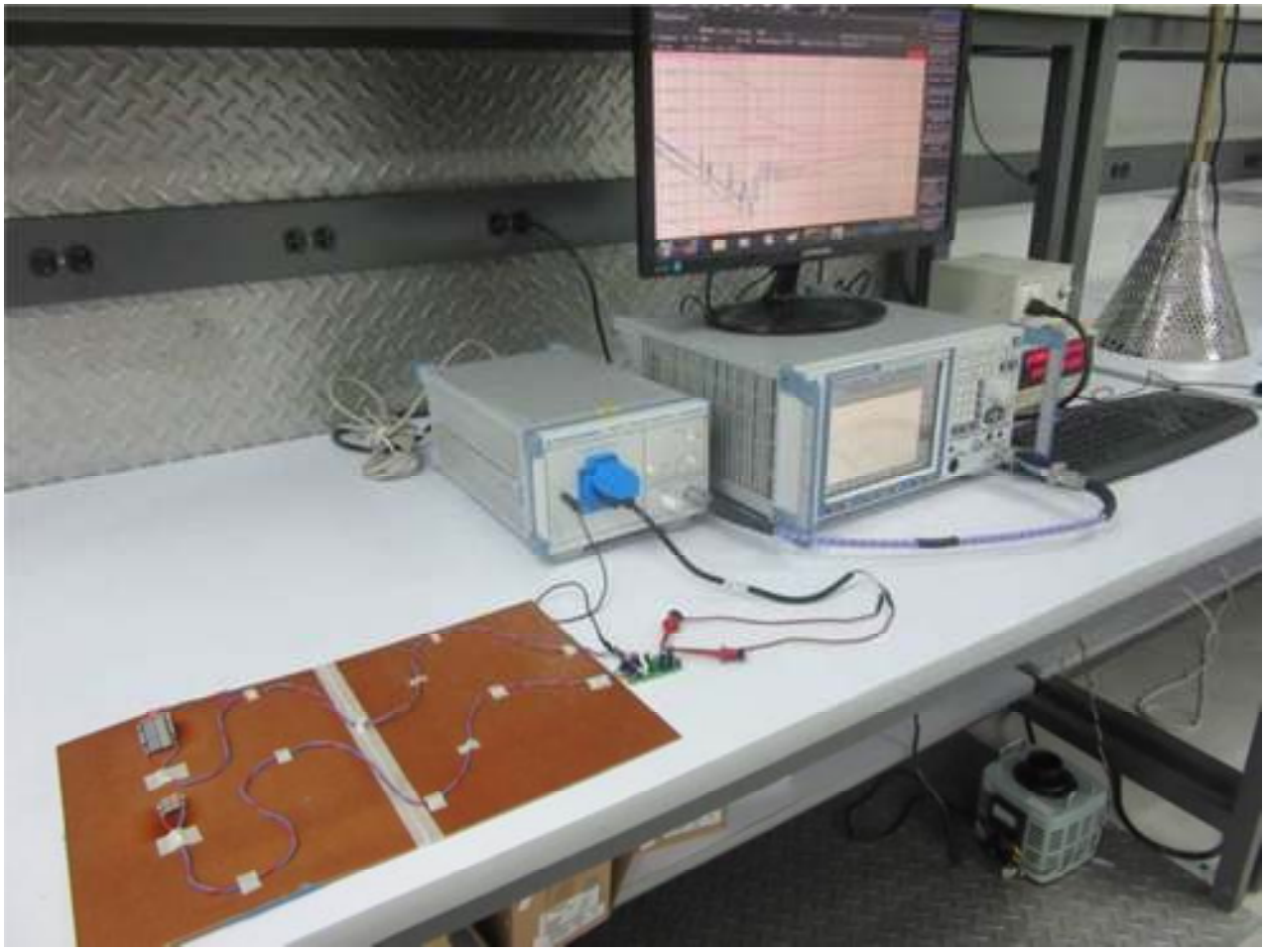

Figure 46 – EMI Test Set-up.

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12.2 Floating Output (QP / AV)

12.2.1 Line 115 VAC

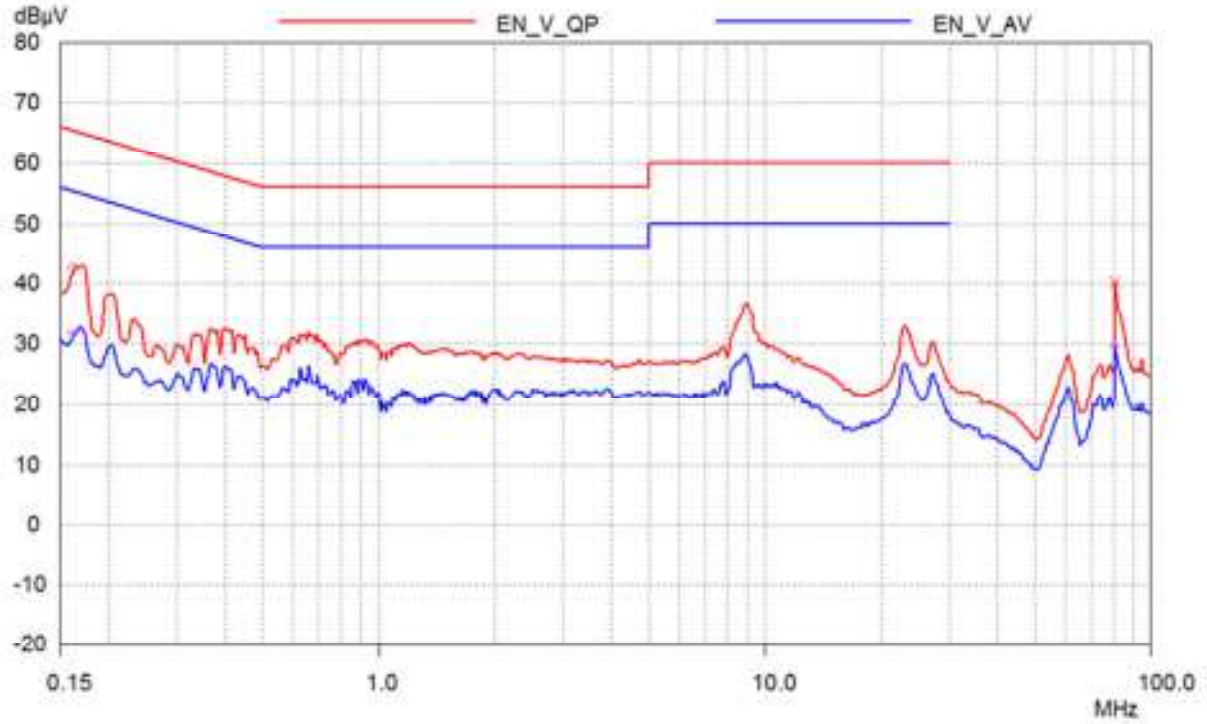

Figure 47 – Floating Negative Output at 115 VAC, Line.

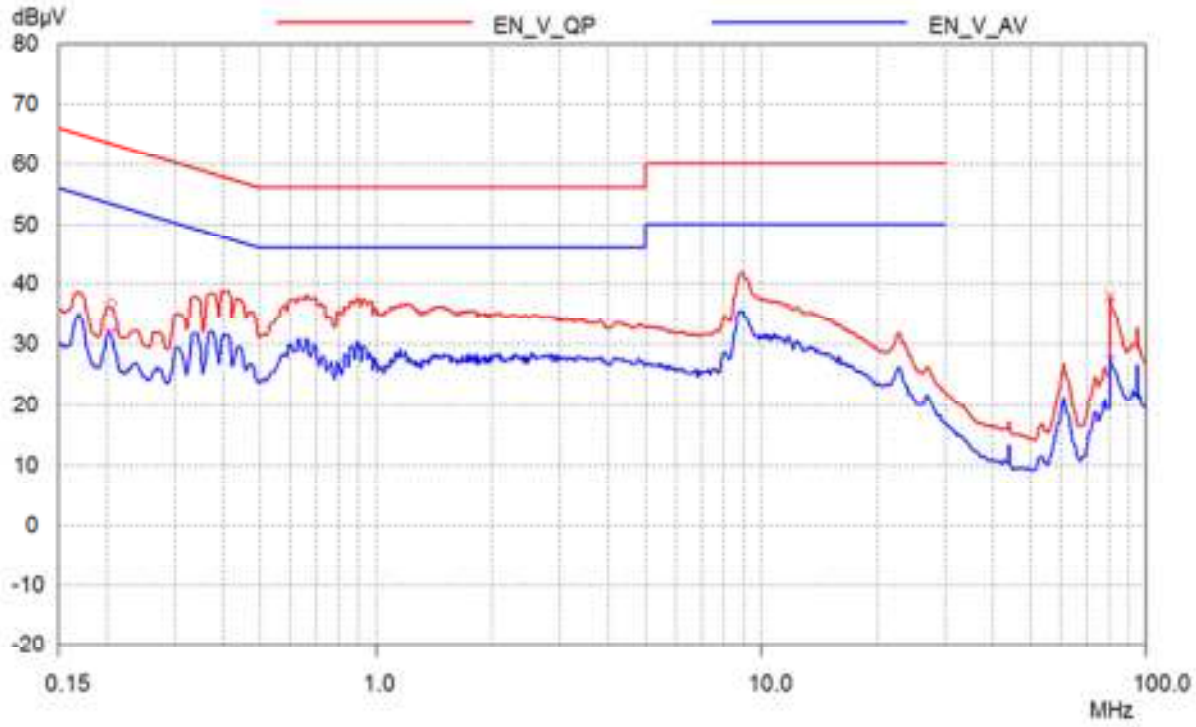

Figure 48 – Floating Negative Output at 115 VAC, Neutral.

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12.2.2 Line 230 VAC

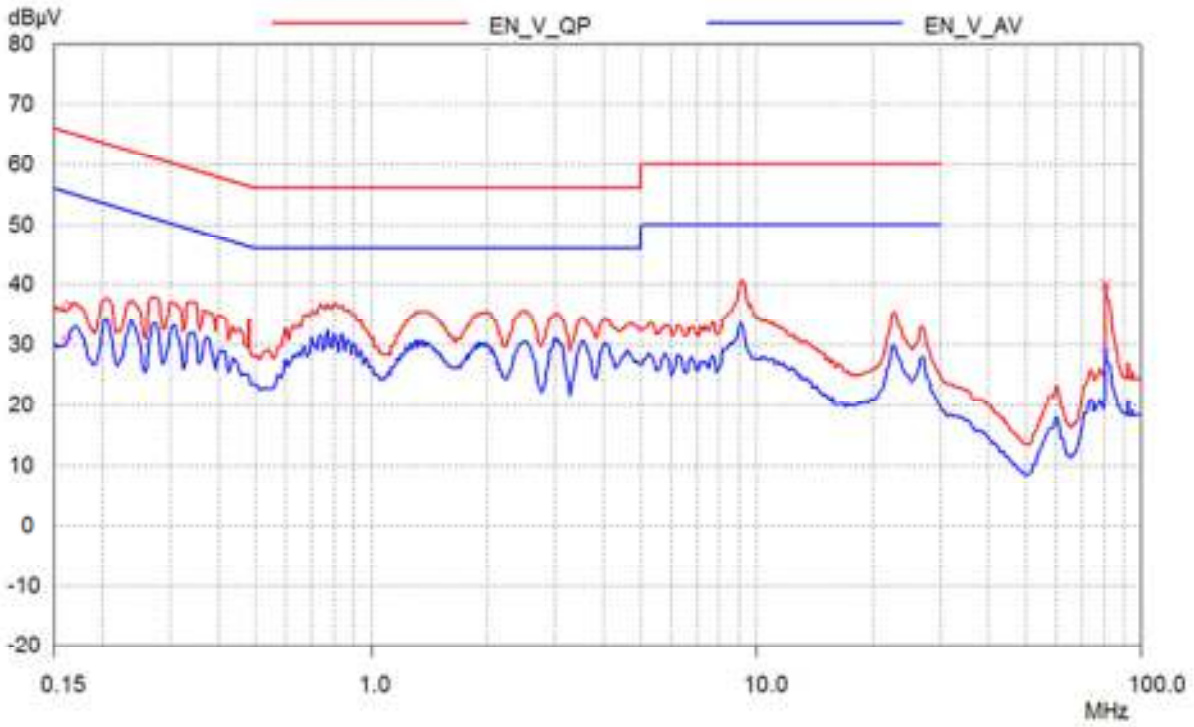

Figure 49– Floating Negative Output at 230 VAC, Line.

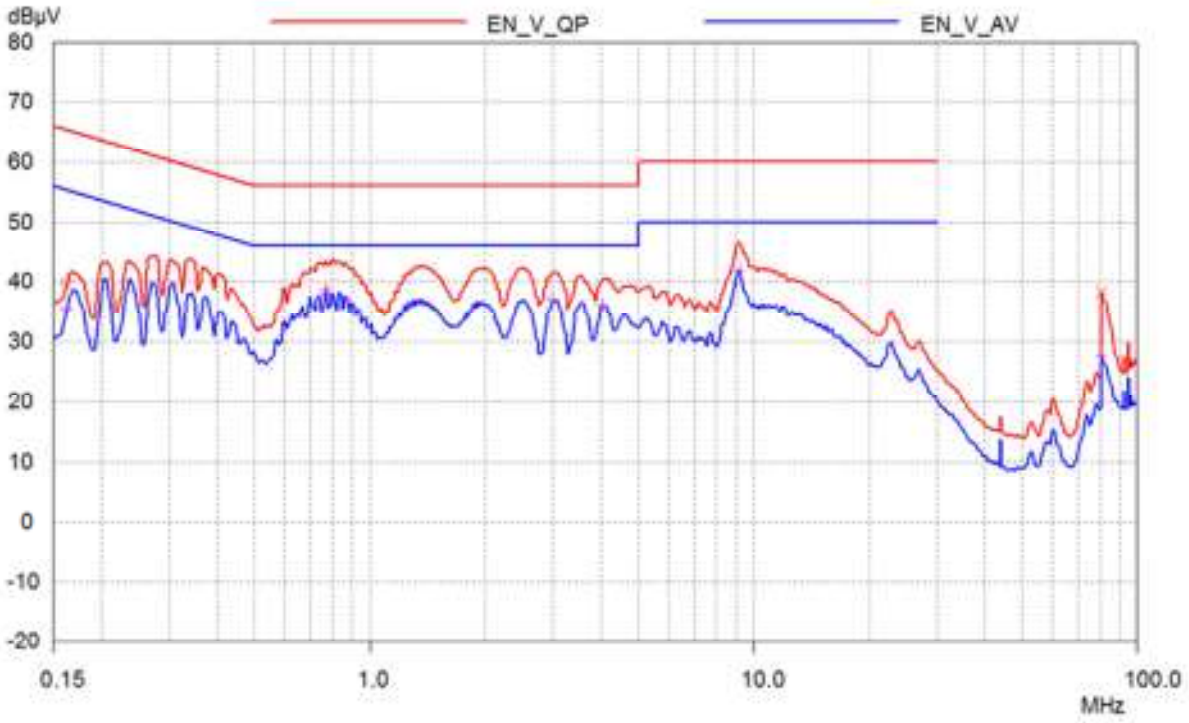

Figure 50 – Floating Negative Output at 230 VAC, Neutral.

Test condition: 4.75 W (18 V full load, 5 V full load)

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13 Lightning Surge Test

The unit was subjected to ±1000 V, differential surge using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

13.1 Differential Mode Surge Test

Passed ±1 kV

Ring Wave Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
1	0	2	10	PASS
1	90	2	10	PASS
1	180	2	10	PASS
1	270	2	10	PASS
-1	0	2	10	PASS
-1	90	2	10	PASS
-1	180	2	10	PASS
-1	270	2	10	PASS

14 Revision History

Date	Author	Revision	Description & Changes	Reviewed
08-Nov-16	CC & JW	1.0	Initial Release	Mktg & Apps

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